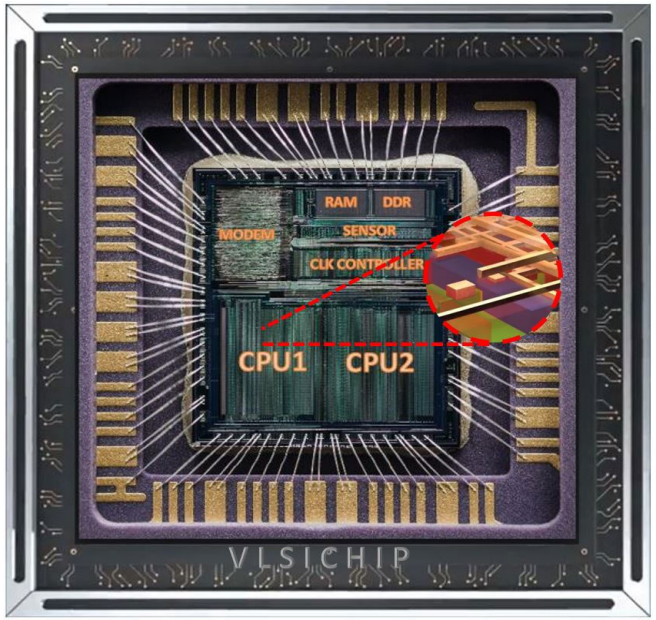
Workshop Outline

Contents

- Introduction to VLSI Backend Flow
- Stages and Sign-off Checks Overview
- OpenROAD Design Flow
- Detailed VLSI Backend Flow
  - RTL Synthesis
  - Floorplanning
  - Placement
  - Static Timing Analysis
  - Clock Tree Synthesis
  - Routing
  - GUI
  - OpenROAD for PPA
- Hands-on
  - Installation of the OpenROAD Tool.
  - Input files
  - RTL synthesis
  - Sanity Checks
  - Floorplan and Placement
  - Post-placement Timing Analysis
  - Clock Tree Synthesis (CTS)
  - Post-CTS Timing Analysis
  - Routing and DRC/LVS Check.

Objective

The objective of this workshop is to train the participants with VLSI design backend flow through the open-source VLSI design tool "OpenROAD". After successful completion of this workshop, the participants would be able to run the RTL synthesis to GDS-2 flow for their own design.



IIT Guwahati
in association with
Ministry of Electronics and Information Technology

ELECTRONICS INDIA
Billion Needs Million Chips

Workshop on

"OpenROAD for Low-cost ASIC design for Rapid Innovation"

8 JAN– 13 JANUARY 2024
Conference Hall 1 and 4,
Indian Institute of Technology Guwahati, Guwahati - 781039,

Contact:

For queries related to accommodation:
Mr. Ravi Dubey
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Email: piaipqcmeity@iitg.ac.in
Landline No.:0361-258-3182
Time to contact : 9.00 AM to 6.00 PM

Tentative Speakers

Keynote Speaker

Prof. Andrew B. Kahng

Department of Computer Science and Engineering
University of California San Diego

Invited Speakers

Mr. Tom Spyrou, Precision Innovations Inc.
Ms. Indira Iyer, Precision Innovations Inc.
Ms. Sunita Verma, Scientist-G, MeitY
Mr. Nishit Gupta, Scientist-E, MeitY
Prof. V. Kamakoti, IIT Madras
Prof. Madhav Desai, IIT Bombay
Prof. Sachin B. Patkar, IIT Bombay

Expert Talks

Prof. Chandan Karfa, IIT Guwahati
Prof. John Jose, IIT Guwahati
Prof. Sukumar Nandi, IIT Guwahati
Prof. Prithwijit Guha, IIT Guwahati

Outcomes

The workshop on Opensource EDA Design tool, OpenROAD, is organized to bring together researchers, developers, and users to discuss advancements, share knowledge, and collaborate on open-source tools for chip design. After completion of this workshop, participants would be able to design digital circuits through VLSI backend flow.

Who can apply?

Students, researchers, faculty members and industry professionals working in the domain of digital VLSI Design

Participants willing to attend the workshop in the offline mode need to register as early as possible to get on-campus hostel accommodation.

HOW TO APPLY ?

Fees: Student/Research Scholar/Other: Rs. 500
Faculty Member/Industry professional: Rs.1000

For NEFT:
Bank Name: State Bank of India
A/C Name: IIT Guwahati (R&D)
Account No.: 36071160089
IFSC Code: SBIN0014262

Form QR code

Reg. Link: https://forms.gle/hixmUWcVjA3kBbnbA

Note: Participants have to submit UTR No. as the proof of payment while registering to the workshop.

DETAILS

Workshop Duration: 06 Days
Last Date: 5 Jan 2024

Workshop Mode: Hybrid (Online + offline)
It is recommended that participants should carry their own laptop having min. 08 GB RAM and Core i3 Processor

Accommodation and food would be made available only for the offline participants.

Organizing Committee

Prof. Gaurav Trivedi (Convenor)
Prof. Aryabartta Sahu (Co-Convenor)
Prof. Prithwijit Guha
Prof. S. Krishnaswamy
Prof. H. S. Shekhawat
Prof. Harshal B. Nemade
Prof. Pratima Agarwal
Prof. John Jose
Prof. Rohit Sinha
Prof. Sukumar Nandi

Volunteers

Amol Boke, Rupali Jarwal, Feroza Haque, Nilutpal Changkakati, Naorem Yaipharenba Meitei, Vikash Prasad, Shailesh Chandra Pandey, Raktim Choudhury, Tina Susan Thomas, Taniya Salotra, Avula Manoj Kumar Reddy, Rushik Parmar, Divya Nakerakanti, Abhyuday Bhardwaj, Akash Dev Roshan, Saras Mani Mishra, Ankita Tiwari, Bipul Boro, Parmita Roy, S.S.P. Goswami, Subhadip Poria, Aditi Chakraborty, Nitin M., Sachin Kumar