

## Research and Development Section Indian Institute of Technology Guwahati Guwahati-781039, Assam

Applications are invited for an **online interview** for the following post(s) in the project entitled, **"SMART CONTACTLESS TECHNOLOGY DEVELOPMENT FOR SMART FENCING"** at the department of Electronics and Electrical Engineering, IIT Guwahati.

Date: 16 Apr 2021 (Friday)

Time: 11.00 AM

Venue: MS Teams or Google Meet (Link will be posted on the link http://www.iitg.ac.in/trivedi/

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1		JRF (GATE)	1	31000	Yes Rs. 4960	1250	37210.00		BTech/MTech or PhD in EC/EE/CS with valid GATE Score, whereas BTech (EC/EE/CS with valid GATE Score) with minimum TWO years of work experience in VLSI SoC design is desired for the position of JRF. Candidates with the knowledge of Verilog / System Verilog / FPGA based system design / EDA tools (Synopsys / Cadence / Siemens-Mentor) would be preferred. Candidates are expected to have experience on complete VLSI SoC design flow and chip tapeout using commercial EDA tools.

**How to apply and selection process:** Candidates have to appear in the online interview along with an application / CV on plain paper giving details of all educational qualifications, experience, contact address, phone no., E - mail etc. and send to the Principal Investigator before 16 Apr 2021 (Friday).

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Selection will be based on the performance of the candidate in the interview. Candidates will not be sent any call letter separately. Advance copy of CV may be sent to the Principal Investigator.

For any clarification, contact: Gaurav Trivedi (Principal Investigator)

Email: trivedi@iitg.ac.in Phone: 8011000783

No campus accommodation will be available for the selected candidates. No TA/DA will be paid to the candidates for appearing in the test and interview.

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