Corrigendum

Against our NIQ No. **IITG/RND/T118R/23-24** and Tender ID: 2024_IITG_792231_1 the following changes has been made.

(1) Due to typo error in uploaded BOQ, the following changes may be considered:

(a) **Item 1.01 (Zynq UltraScale)** should be treated as **Zynq UltraScale+ MPSoC ZCU102 Evaluation kit**,

(b) **Item 1.01** (Zynq UltraScale+ MPSoC ZCU102 Evaluation kit)-
Software Module: 1 user ML Enterprise Edition, Vitis Model Composer, Software must be compatible with FPGA boards for FPGA design and programming. Software must have perpetual academic license along with the boards.

(c) **Item 1.02 (MPSoC ZCU102 Evaluation kit)** should be treated as **NVIDIA Jetson AGX Orin Developer Kit.'**

(2) Last date of bid submission now to be read as 12.02.2024 (12.00hrs) instead of 08.02.2024 (12.00 hrs).

(3) Bid opening date now to be read as 13.02.2024 (14.00hrs) instead of 09.02.2024 (14.00 hrs).

Sd/-
AR(R&D)