International Workshop on Design Principles for Next Generation Embedded Computing Systems

(5th - 8th July & 12th - 13th July, 2021)

(Under the SPARC Project 'Approximate Computing Techniques for Resource Constrained Edge Devices')

Resource Person:
Dr. Amit Singh
School of Computer Science and Electronic Engineering
University of Essex, UK

Workshop will be conducted in online mode.
Dates: 5th – 8th July, 2021 and 12th – 13th July, 2021
Time: 11:30 AM – 1:30 PM (IST)
[Total 12 hours: 6 days, 2 hours each]

Workshop Contents

- **Introduction to embedded systems**
- **Multi-core based next generation embedded systems**
- **Applications execution on next generation embedded systems**
- **Important metrics for embedded systems**
- **Design-time optimisation principles for various metrics**
- **Run-time time optimisation principles for various metrics**
- **Online programming demonstration for a multi-core based embedded system**
- **Envisioned future and design challenges for next generation embedded systems**

Resource Person Profile [https://www.essex.ac.uk/people/singh42308/amit-singh]

Dr. Amit Kumar Singh is an Associate Professor at University of Essex, UK. He received the B.Tech. degree in Electronics Engineering from Indian Institute of Technology (Indian School of Mines), Dhanbad, India, in 2006, and the Ph.D. degree from the School of Computer Engineering, Nanyang Technological University (NTU), Singapore, in 2013. He was with HCL Technologies, India for a year and half until 2008. He has a post-doctoral research experience for over five years at several reputed universities. His current research interests are design and optimisation of multi-core-based computing systems with focus on performance, energy, temperature, reliability and security. He has published over 100 papers in reputed journals/conferences, and received several best paper awards, e.g. IEEE TC February 2018 Featured Paper, ICCES 2017, ISORC 2016, PDP 2015, HiPEAC 2013 and GLSVLSI 2014 runner up. He has served on the TPC of IEEE/ACM conferences like DAC, DATE, CASES and CODES+ISSS.

For more details, visit the workshop website: https://www.iitg.ac.in/johnjose/sparc3.html

Who are eligible?
(1) UG, PG and Ph.D students & faculty of CSE/ECE/EEE/IT branches.
(2) Personnel from industry and R&D firms who are interested in this domain.

E-certificates will be provided to participants who attend all sessions of the workshop.
No Registration Fee | Limited seats | Last date for registration: 28.06.2021

Registration Form link: https://tinyurl.com/7ddduhm6

Publication of provisional list of selected candidates on workshop website : 29.06.2021
Publication of final list of confirmed candidates on workshop website : 01.07.2021
Shortlisted candidates need to confirm their participation to receive the link for online sessions.

Programme Coordinators:
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