International Workshop on
Design Principles
for Next Generation Embedded Computing Systems

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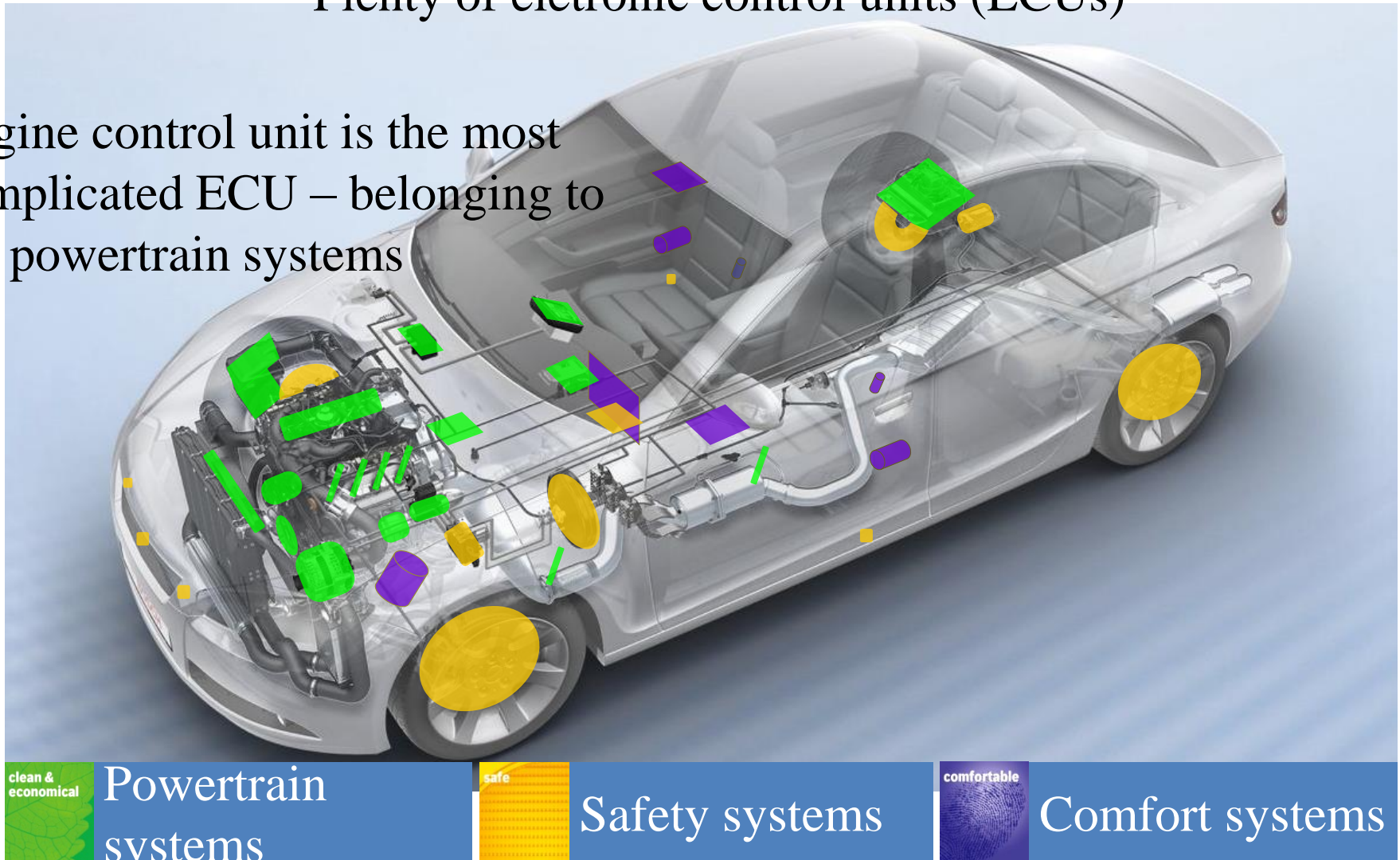W: http://aksingh.co.uk/   E: a.k.singh@essex.ac.uk

Genetic Algorithm (GA) with an Example
(considering both Mapping and DVFS)

Automotive Technology

Plenty of eletronic control units (ECUs)

Engine control unit is the most complicated ECU – belonging to the powertrain systems
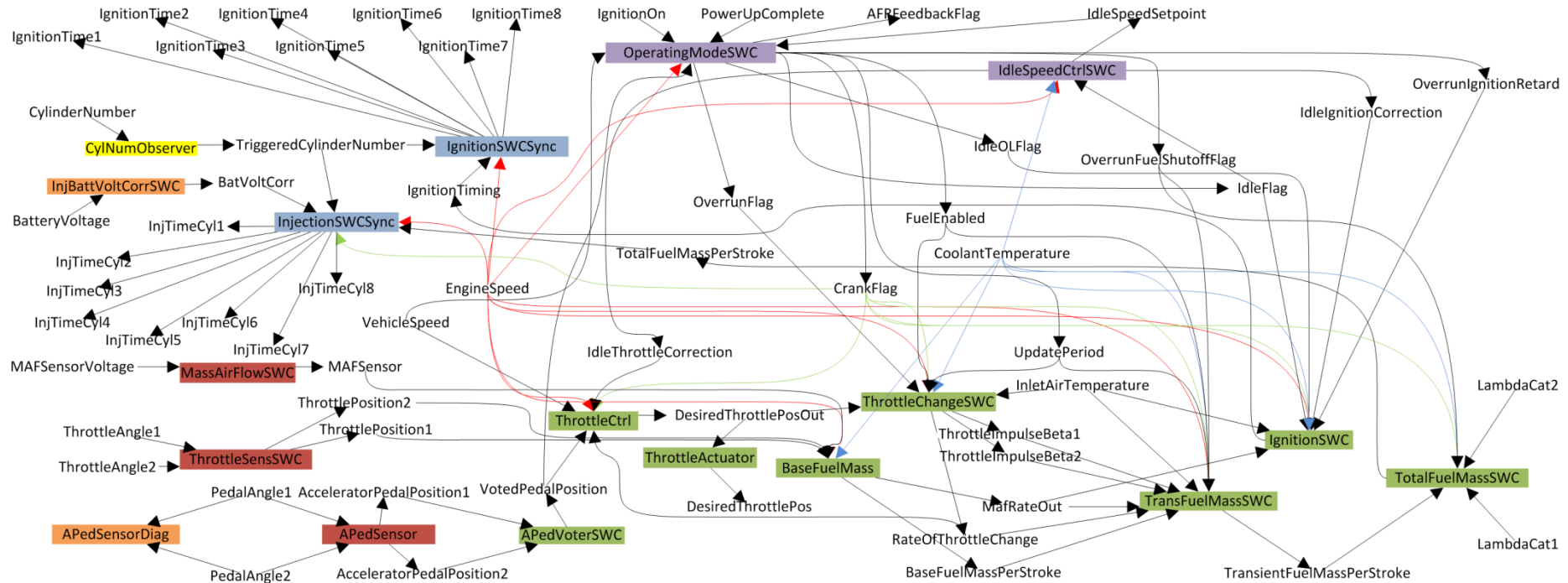

| clean & economical | Powertrain systems | safe | Safety systems | comfortable | Comfort systems |

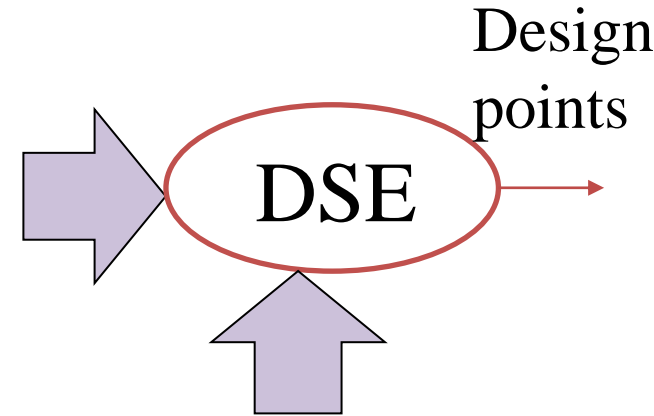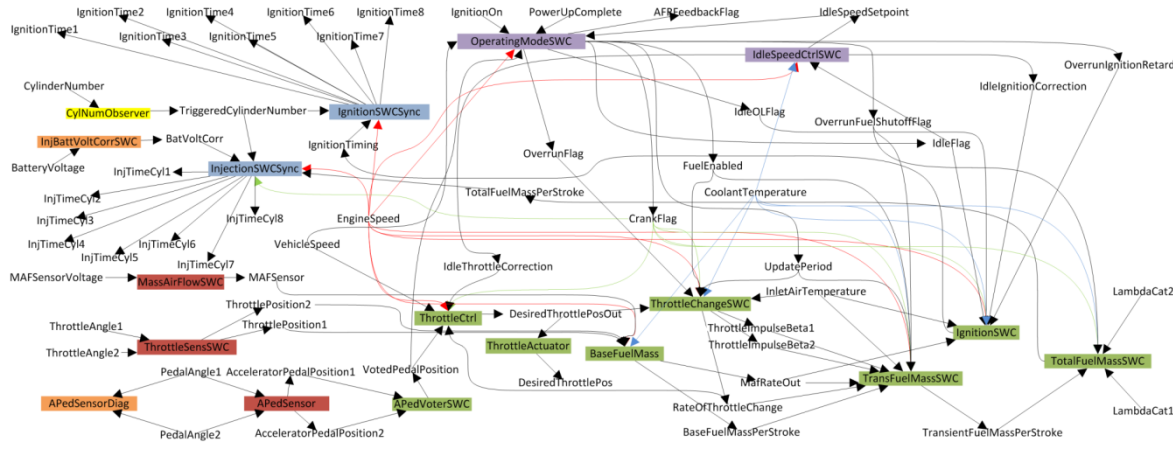Source: Robert Bosch GmbH, Future mobility: automated, connected, electric, Belgian Insurance Conference, 2017

DemoCar- Minimal functionality gasoline Engine Control Unit

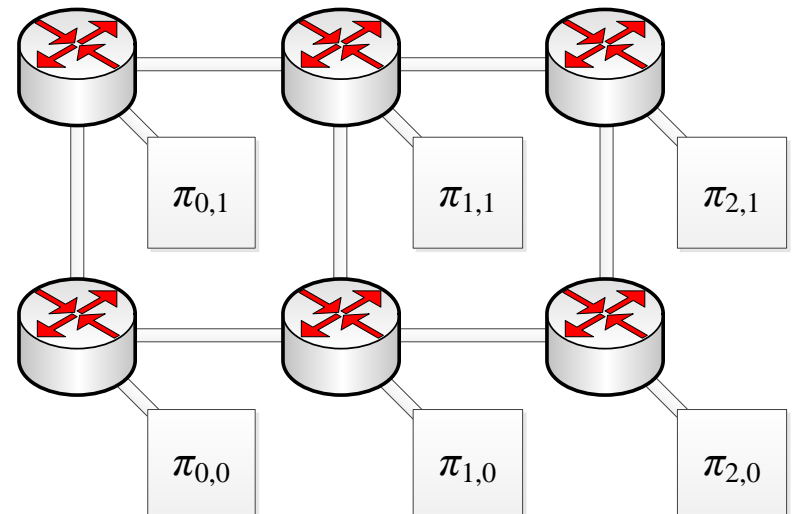

- 18 runnables

- 6 tasks

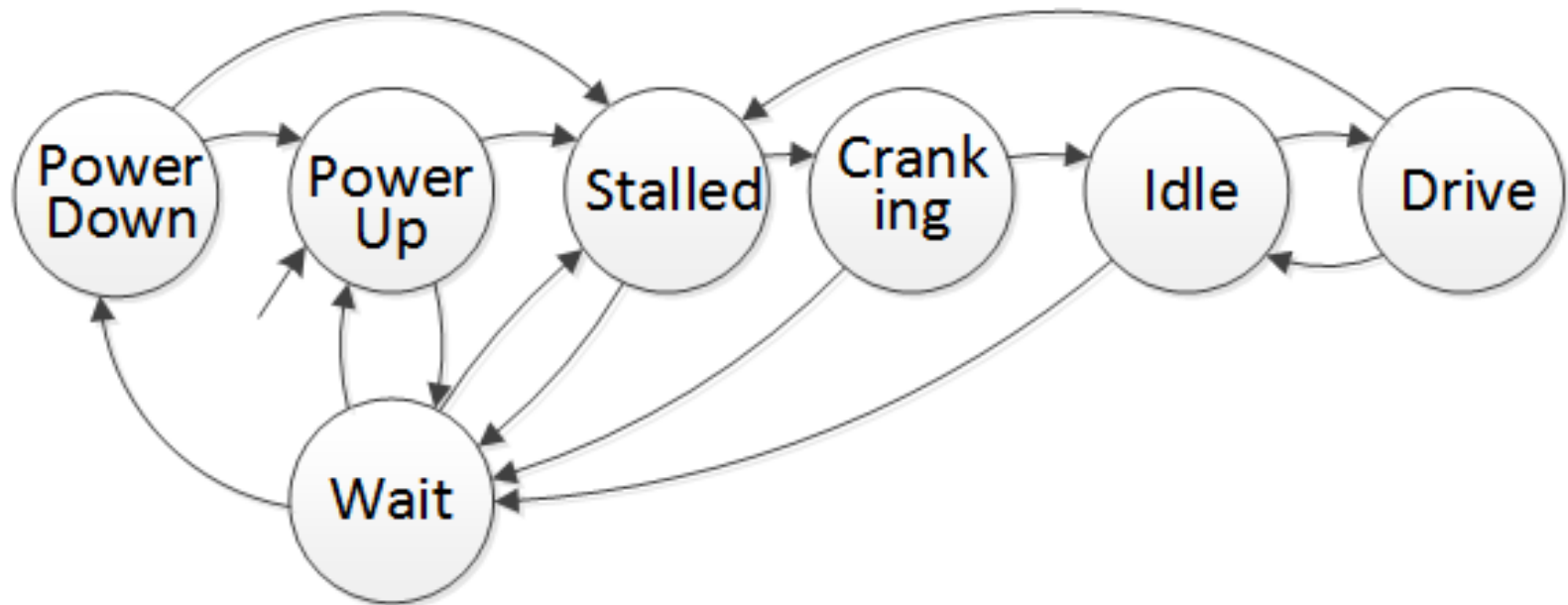- 61 labels (data elements that can be read or written by runnables)

Design-time DSE

Design points

DSE

Possible Goals:
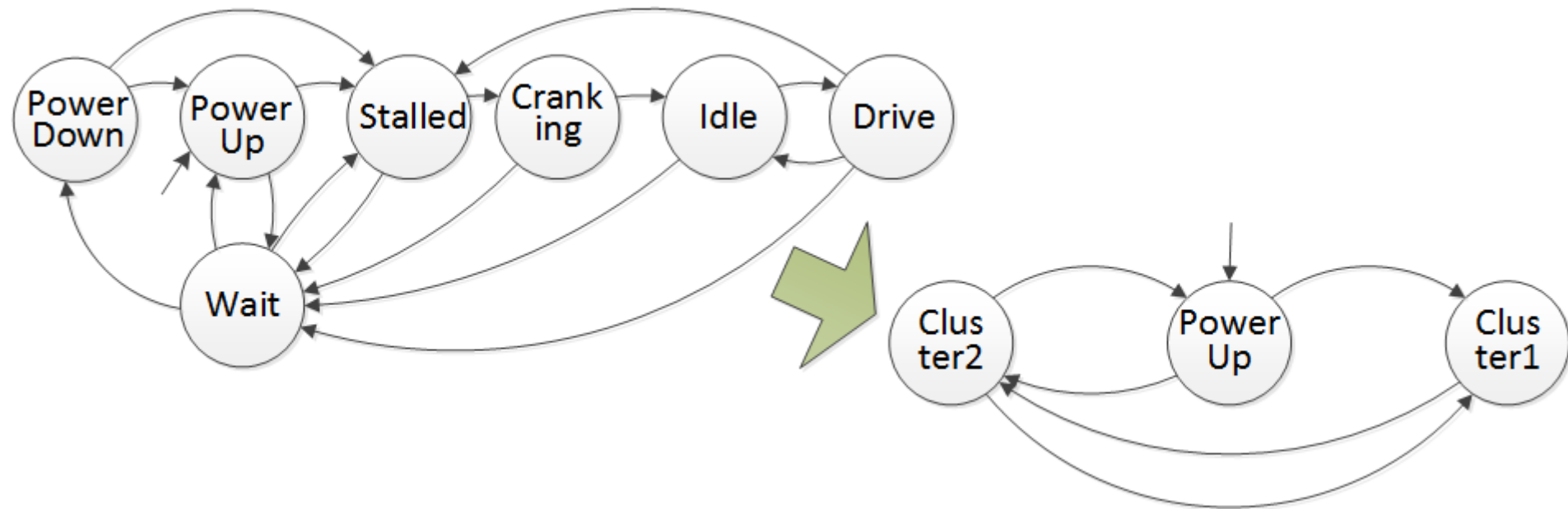- no deadline violation
- minimal #used resources
- minimal energy dissipation

$\pi_{0,1}$ $\pi_{1,1}$ $\pi_{2,1}$

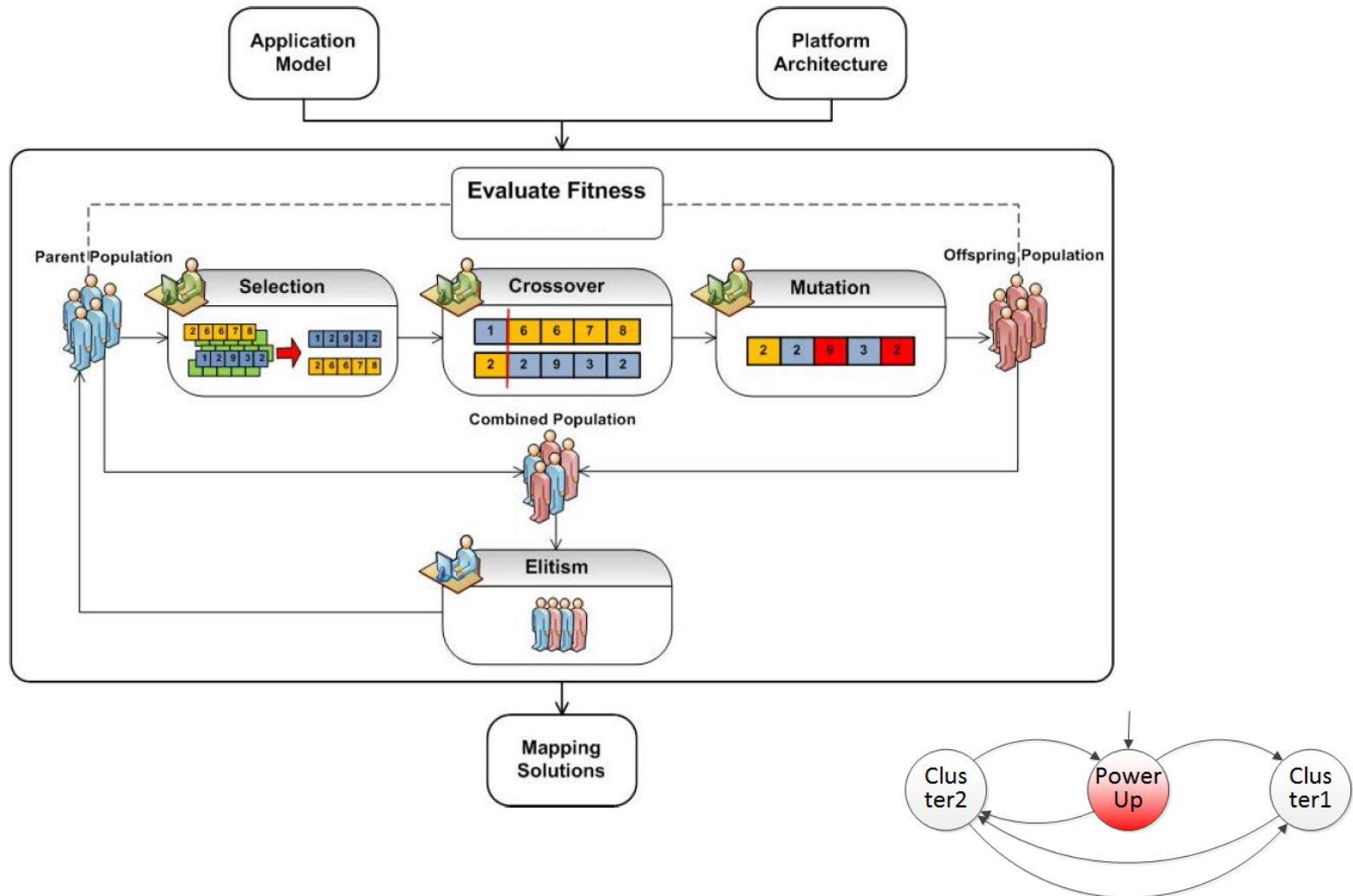$\pi_{0,0}$ $\pi_{1,0}$ $\pi_{2,0}$

The runnables behave differently depending on the state

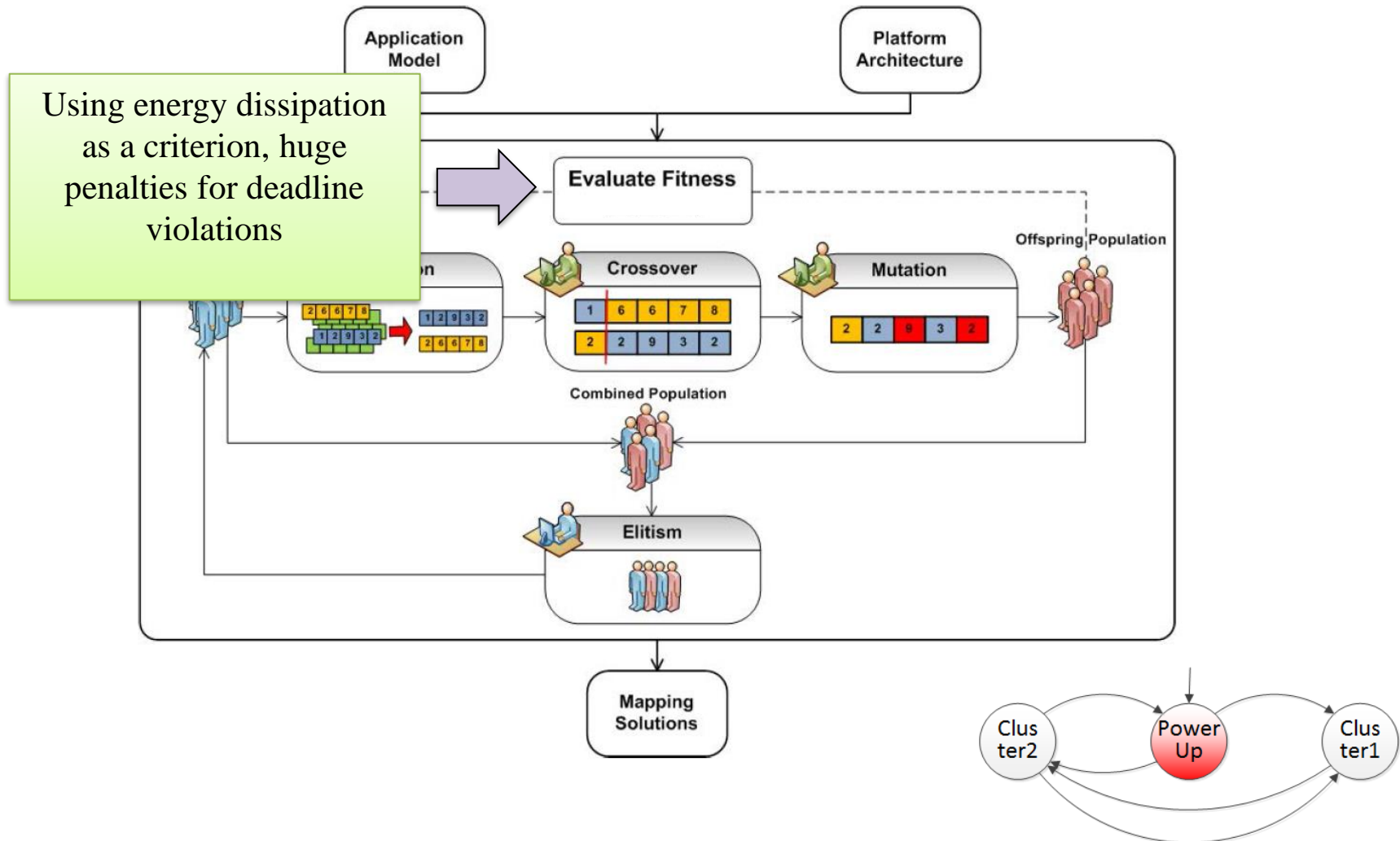# Mode clustering

- To avoid time consuming frequent contexts migration during runtime.
- Some neighbouring modes can have similar runtime and resource consumption, so better to cluster them

GA – for a mode

GA – for a mode

Using energy dissipation as a criterion, huge penalties for deadline violations

Genes in chromosomes
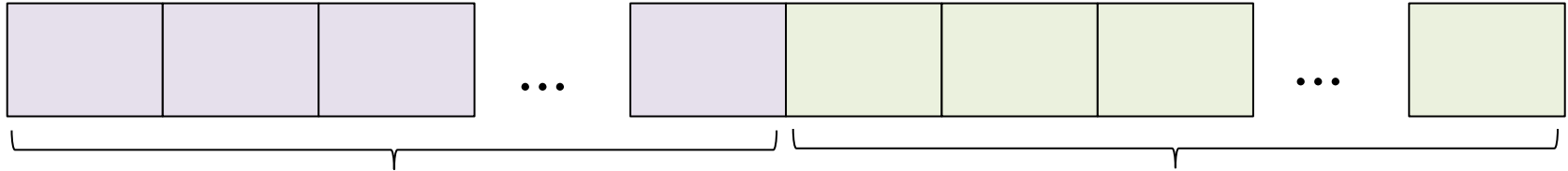
Runnable mapping (n genes)   Core P-mode (x·y genes)
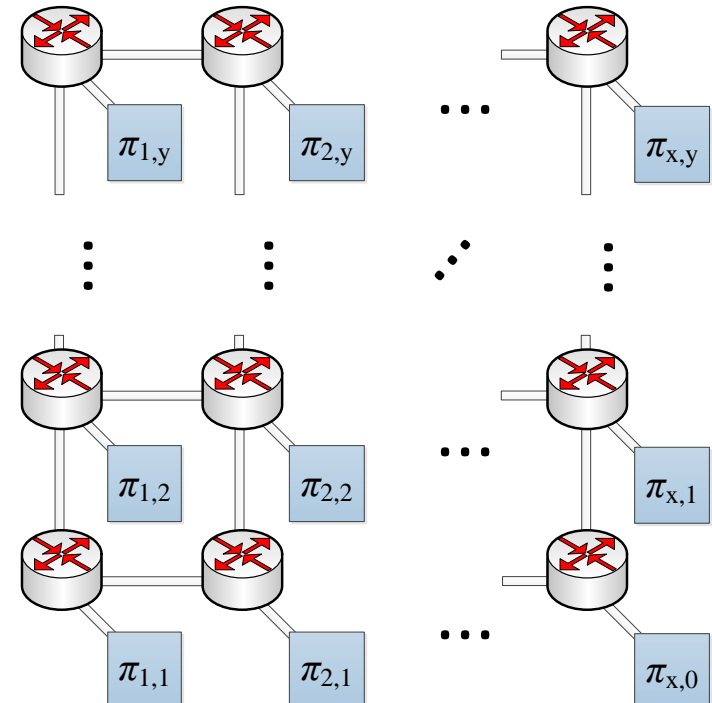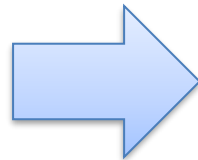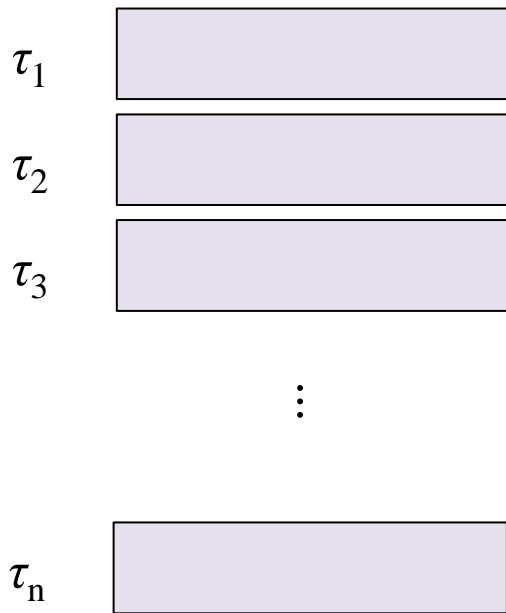
Will you always get optimal design-point when using GA?

No

Yes

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Optimization results

- **Energy-aware Resource Allocation in Multi-mode Automotive Applications with Hard Real-Time Constraints**
  Piotr Dziurzanski, <u>Amit Kumar Singh</u>, Leandro Soares Indrusiak
  IEEE International Symposium on Real-Time Computing (ISORC), York, UK, May 2016.
  Best Paper Award

- **Hard Real-time Guarantee of Automotive Applications during Mode Changes**
  Piotr Dziurzanski, <u>Amit Kumar Singh</u>, Leandro Soares Indrusiak, Björn Saballus
  ACM International Conference on Real-Time Networks and Systems (RTNS), Lille, France, November 2015

- **Benchmarking, System Design and Case-studies for Multi-core based Embedded Automotive Systems**
  Piotr Dziurzanski, <u>Amit Kumar Singh</u>, Leandro Soares Indrusiak
  International Workshop on Dynamic Resource Allocation and Management in Embedded, High Performance and Cloud Computing (DreamCloud), co-located with the HiPEAC, Prague, Czech Republic, January 2016.

- ………

Can we employ similar GA procedure for any application represented as task graph?

No

Yes

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DSE for Multi-threaded Applications

Applications on Heterogeneous Multi-core CPUs

Samsung Exynos 5422 SoC

Cortex-A15 cluster		Cortex-A7 cluster		GPU
Core$_0$	Core$_1$	Core$_0$	Core$_1$	ARM Mali-T628
Core$_2$	Core$_3$	Core$_2$	Core$_3$	
2MB L2-Cache		512KB L2-Cache		128KB L2-Cache

128-Bit AMBA ACE BUS interface

2GB DRAM
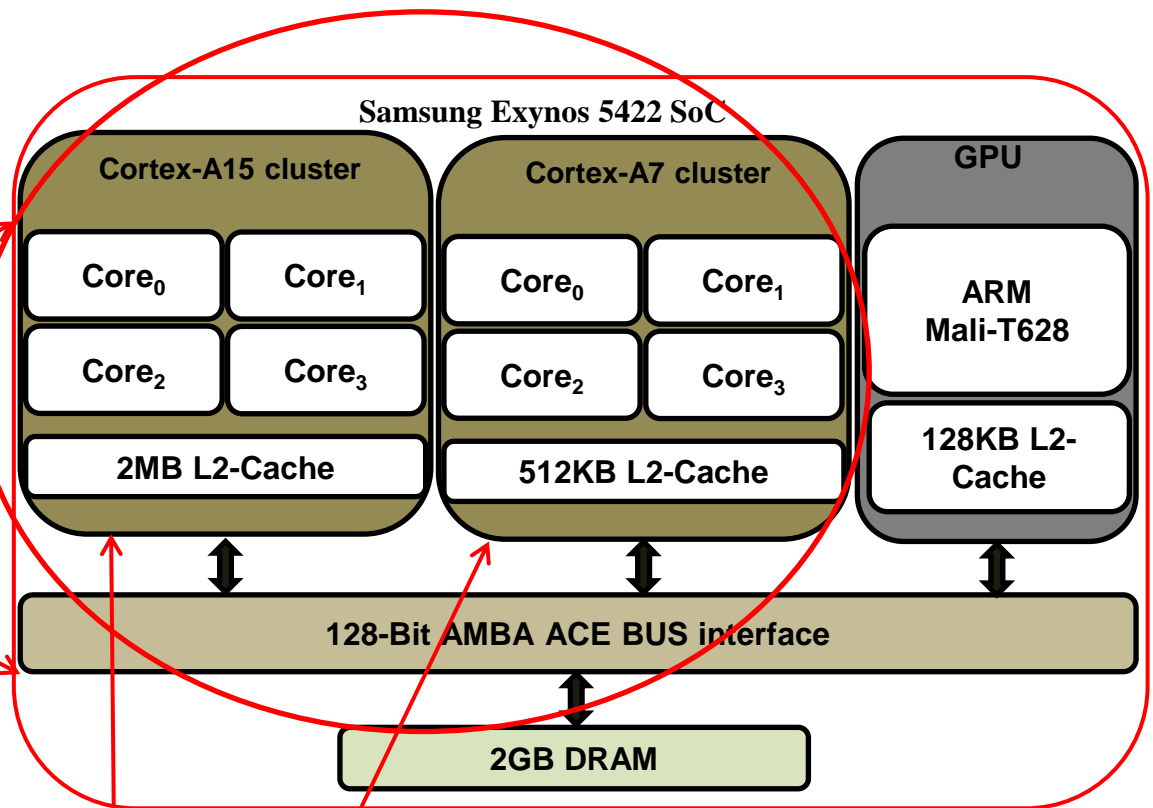
big   LITTLE

Blackscholes – Time and Energy
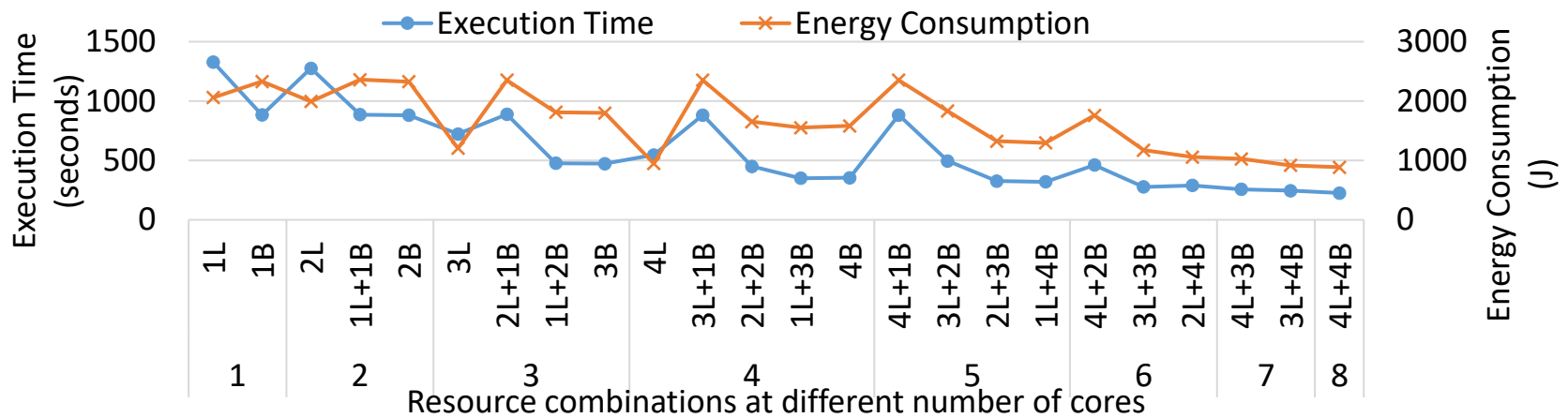
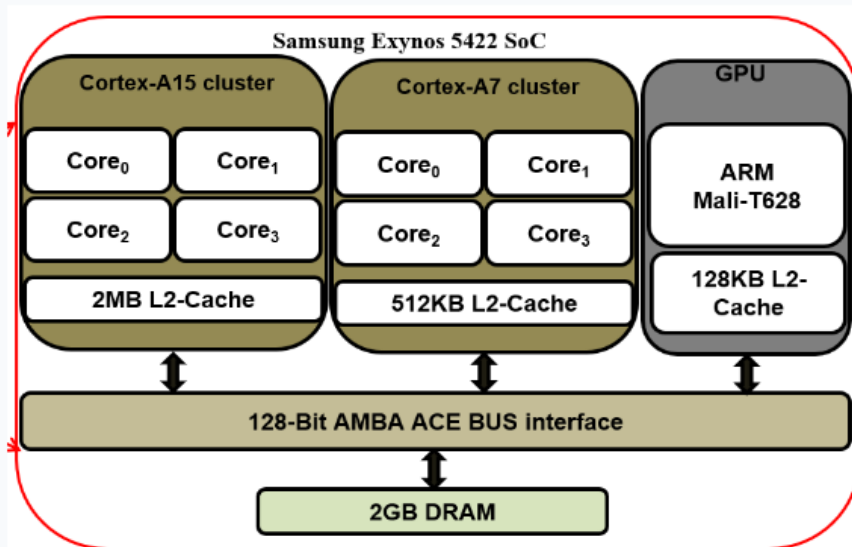# Number of design points when big cluster has 2 frequency levels LITTLE has 3 frequency levels?

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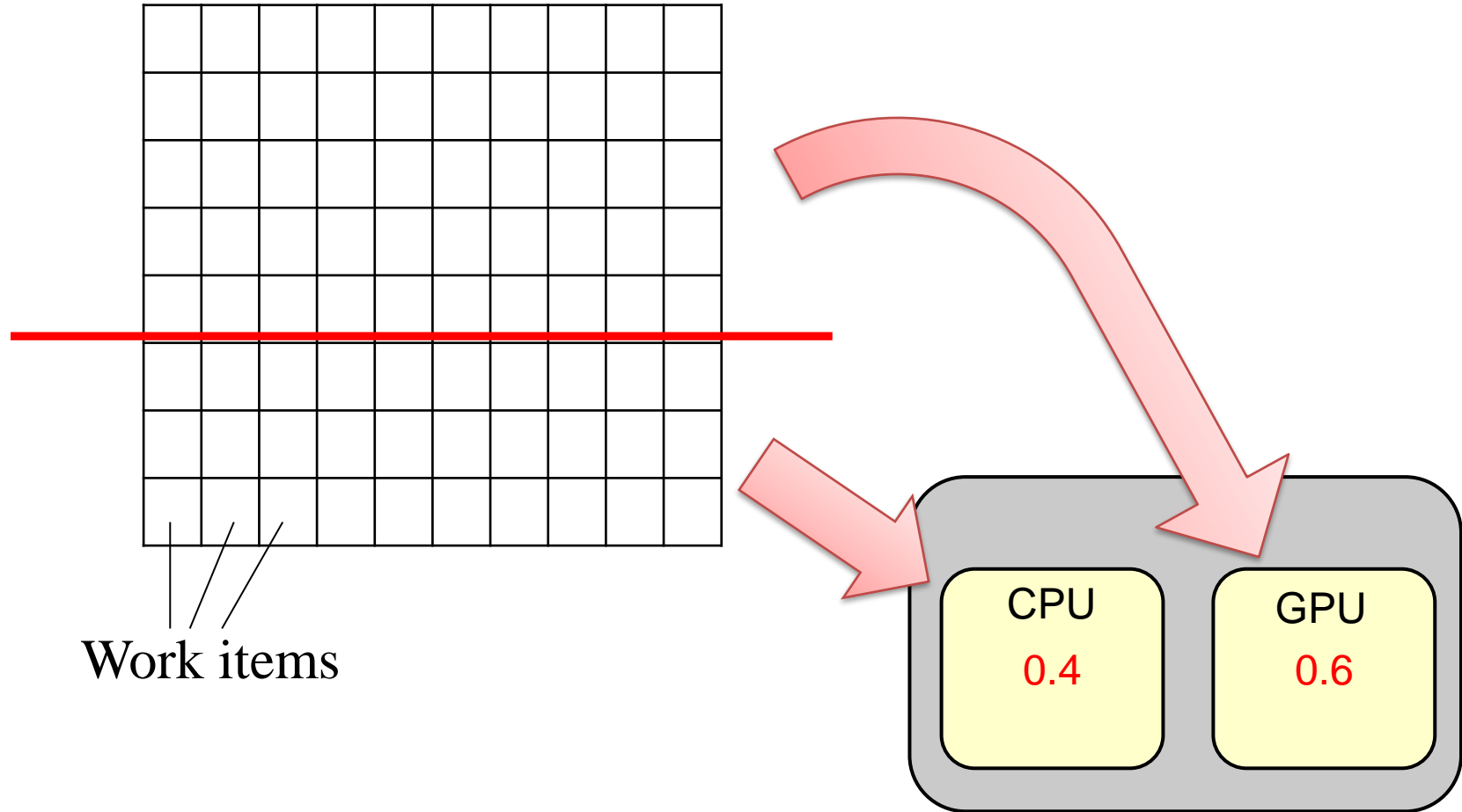
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Total Design Points (TDP)

$$TDP = \{(N_b \times F_b) + (N_L \times F_L) + (N_b \times F_b \times N_L \times F_L)\}$$
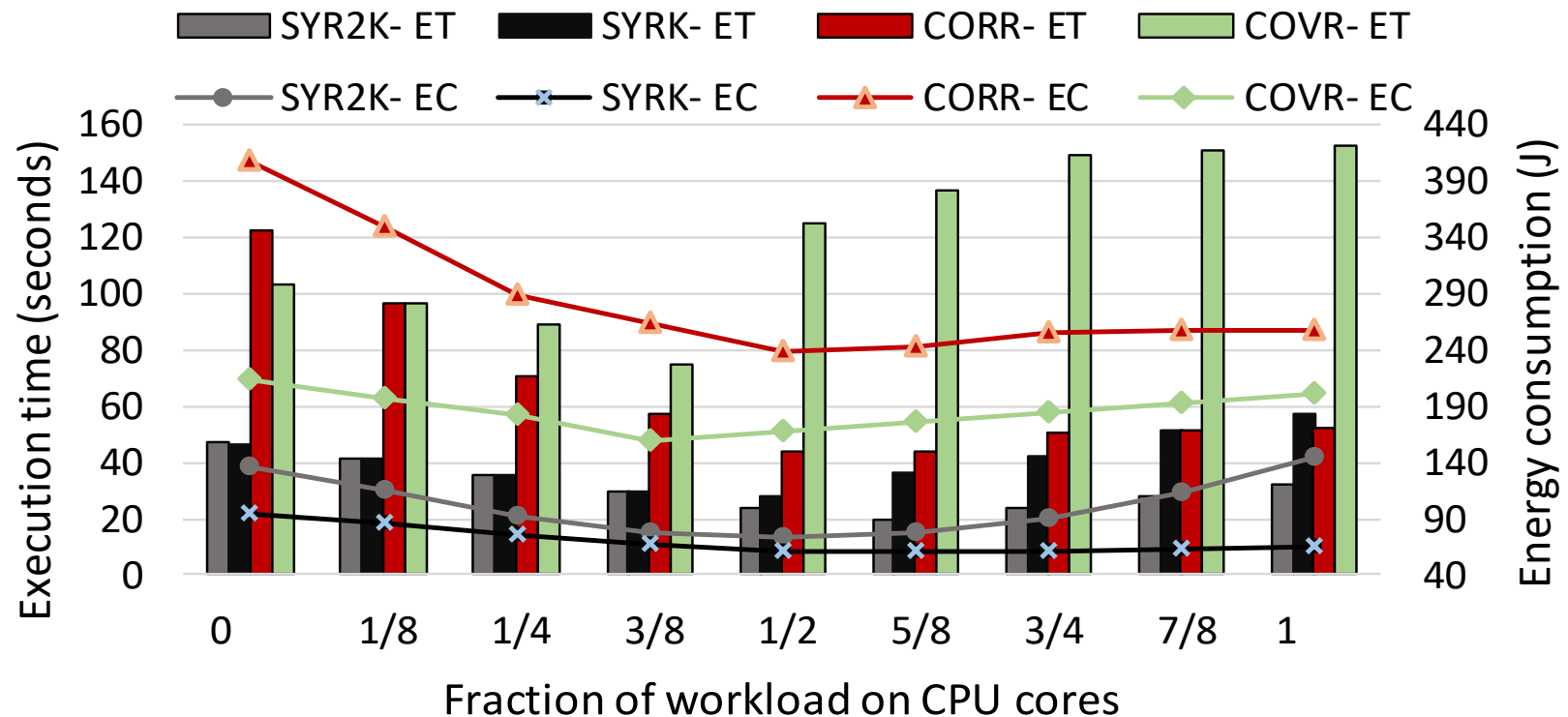
- So, you can compute now.

Partitioning for Single (data-parallel) Application

Work items

CPU
0.4

GPU
0.6

OpenCL provides this opportunity

Partitioning Results: Time and Energy

- Some applications execute faster on CPU cores than GPU cores (e.g., CORR),
- All applications show a significant reduction in execution time and energy consumption when run on both the CPU and GPU cores, with an appropriate fraction value

Design-time Optimization (DSE) – Other aspects

- **Other metrics, e.g. temperature, reliability and security can also be evaluated for each design point.**

- **Other control knobs, e.g. routing, cache/memory optimisation, processor customisation, etc. can also be considered.**

What is disadvantage of design-time optimisation (DSE)?

Incurs high computation cost.

Extensive pruning may result in sub-optimal solutions.

Not suitable for run-time varying workloads in the systems.

All of the above.

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Run-time Optimisations

-> Next Topic

Questions?