Scheme for Promotion of Academic and Research Collaboration

International Workshop on Embedded System Technologies for Deep Learning and Approximate Computing

(29 - 30 May & 5 - 6 June, 2021)

(Under the SPARC Project 'Approximate Computing Techniques for Resource Constrained Edge Devices')

Resource person:

Dr.Alessandro Cilardo
Department of Electrical Engineering and Information Technologies
University of Naples Federico II, Italy

Workshop [total 12 hours] will be conducted in online mode.
Date: 29-30 May & 5-6 June, 2021.
Time: 11.30am - 1.00pm, 1.30pm - 3.00pm (IST),

Topics to be covered

Microcontrollers and Application processors	ARM ecosystem: Processor families and evolution of the ARM architecture
Introduction to ARM Cortex-M architecture	System-on-Chip technologies based on ARM Cortex-M
A case-study: STM32 SoC devices	Software development and debug tools, GNU toolchain
ARM CMSIS framework	CMSIS Neural Network library (CMSIS-NN)
Real-Time Operating Systems	A case-study: FreeRTOS
Introduction to ARM Cortex-A architecture	ARM Cortex-A software stack
Hardware-customizable FPGA-based SoC	Case-study: Xilinx Zynq-7000 SoC architecture
An overview of Xilinx FPGA design flows	FPGA-based customized hardware acceleration and opportunities for Approximate Computing

Resource Person Profile [http://www.cilardo.info/ * https://tinyurl.com/58s3h4cp]

Dr. Alessandro Cilardo is an associate professor with the University of Naples Federico II. He received a five-year degree in Electronics Engineering cum laude, in 2003, and a PhD degree in Computer Science in November 2006. He is the single or main author of around 90 peer-reviewed papers published in leading scientific journals and conferences, including various IEEE and ACM transactions, as well as top conferences like DATE and FPL. His research focuses on computer architecture, digital design methodologies, computer arithmetic as well as security and cryptography-related processing. He is involved in a number of funded projects at both the national level and the European level (7FP and H2020 projects). He is a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE) and the European Network of Excellence on High Performance and Embedded Architecture and Compilation (HiPEAC).

For more details, visit the workshop website: https://www.iitg.ac.in/johnjose/sparc1.html
Who are eligible? (1) UG, PG and Ph.D students & faculty of CSE/ECE/EEE/IT branches.
(2) Personnel from industry and R&D firms who are interested in this domain.
Registration link: https://tinyurl.com/55m2rh2p
E-certificates will be provided to participants who attend all sessions of the workshop.
No Registration Fee | Limited seats | Last date for registration: 26.05.2021

Programme Coordinators:
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