DoLaR: Double Layer Routing for Bufferless Mesh Network-on-Chip

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***Abstract*—Network on Chip (NoC) is embraced as an interconnect solution for the design of large tiled chip multiprocessors (TCMP). Bufferless NoC router is a promising approach due to its simple router design, energy and hardware efficiency. NoC, which rely on underlying network architecture, is characterized by performance measures like latency, deflection rate, throughput and power. In this paper, we come up with DoLaR architecture to raise performance of standard bufferless 2D mesh NoC by stacking two similar layers of 8x8 meshes one above the other. DoLaR employs standard 5-port bufferless router architecture and the unused ports of edge routers are utilized to make vertical interconnections between the layers. Simulation results show that our proposed design surpasses existing state-of-the-art 5-port 2D mesh and torus bufferless router designs in terms of better network saturation point and minimized deflection rate, average flit latency and power consumption.**

***Index Terms*—Network-on-Chip, buffer-less, deflection routing, flit latency**

I. Introduction

The recent developments in IC technology have led to massive growth in transistor integration due to the plunge in transistor sizes to ultra-deep submicron levels. This has led to emergence of complex System-on-Chip (SoC) where several IP (Intellectual Property) cores are interconnected by traditional point to point or shared bus intercommunication structures. Network-on-Chip (NoC) has evolved as the preferred communication framework to deal with technology scaling related problems such as global wire delay issue and SoC integration limitations. Modular topology, built-in fault tolerance, better parallelism, scalability, load handling ability and performance over traditional on-chip interconnect solutions make NoC the preferred communication solution for TCMP design [1] [2] [3].

NoC, a packet-switched network, consists of a number of processing nodes in a single chip. TCMP generally uses 2D mesh network architecture owing to its regularity and scalability. Traditional Virtual Channel (VC) based NoC network uses buffers at their input ports to improve throughput and load handling ability of the network. The growing power and area concerns linked with VC based NoC routers are overcome by alternate design choice like bufferless NoC deflection routers. For low and medium injection rates, experimental results show that bufferless deflection router performance surpasses VC based NoC [4]. The flits which are not able to acquire desired output port in bufferless routers will be deflected through an available output port causing routing inefficiency as some of the flits may have to traverse across non-minimal routes. BLESS (BufferLESS) [4] and CHIPPER (CHeap-Interconnect Partially PErmuting Router) [5] are two major bufferless routers which employ deflection routing.

We propose DoLaR, a new design based on CHIPPER, where two identical layers of 2D mesh network are placed one above the other and employs 5-port CHIPPER router microarchitecture with slight modification in the routing algorithm. On comparing our design against a planar 2D mesh network and 2D torus network employing same number of routers exhibit better throughput, minimal latency, deflection rate, footprint and power dissipation while operating at the same speed as 2D design.

The remainder of this paper is ordered as follows: An outline about the related work is presented in Section II and Section III discusses about motivation for our proposed design. In Section IV, details about proposed design are given. Section V discusses about experimental methodology followed. Results are given in Section VI and finally Section VII concludes the paper.

II. Related Work

Conventional VC routers (VCR) employ buffers at their input ports so that flits can stay in them till they attain a productive port. Complex buffer management circuitry is required in addition to buffers, consuming significant portion of on-chip power and occupying large footprint on the chip [6] [7]. This paved way for alternate low cost NoC designs such as centralized buffer/dynamic buffer allocation [8] [9], buffer bypassing [10] or elimination of buffers as in the case of bufferless routing [11]. In bufferless designs, when the desired output link is unavailable, flits are either discarded [12] or deflected through a freely available output link [4] [5]. All the flits that arrive at input ports of a bufferless router advance through one of the output ports. If more than one incoming flit contends for same output link, only one of them will get desired output link whereas other flits which did not

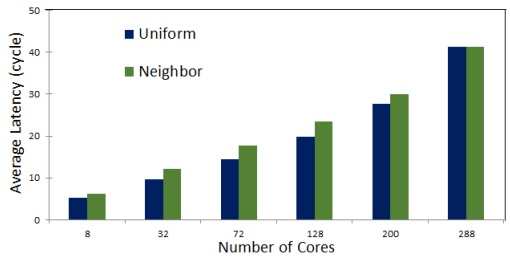

Fig. 1. Average latency versus number of processing cores for different synthetic traffic patterns in 2D mesh bufferless network

get productive links will get deflected through freely available links. Thus network saturates earlier compared to traditional VC routers due to increased flit deflection rate and latency.

The baseline bufferless router, BLESS [4] utilizes a sequential port prioritization mechanism and output port selection employs an age based flit ranking scheme. This leads to reduced NoC operating frequency due to rise in router's critical path delay. CHIPPER [5] is an improvement over BLESS architecture which employs golden packet scheme for packet prioritization and uses parallel port allocation method. In contrast to BLESS, CHIPPER has smaller pipeline stage delay or higher operating frequency but at the cost of increased flit deflection rate since the non-golden flits is pseudo-randomly permuted.

The performance enhancement due to developments in NoC designs is limited due to restricted floor planning alternatives of 2D integrated circuits (IC). Advancements in 3D IC technology have resulted in the migration of 2D NoC based routers to adopt 3D NoC topology. 3D ICs comprises of several active layers of silicon interconnected by short links. 2D NoC networks employ horizontal links created using copper wires. In 3D networks, horizontal connections are made using copper wires and Through-Silicon-Via (TSV) based links are used for vertical interconnections. Better packaging density, noise immunity, minimal power dissipation and improved performance are some of the advantages of 3D IC technology [13] [14].

Li et al. proposes Hybrid 3D NoC-Bus mesh or stacked mesh structure, which is a combination of packet-switched network and bus structure [15]. Improved performance is obtained by replacing standard 7-port 3D NoC router with a 6-port hybrid NoC-Bus 3D switch, which reduces inter-layer distance. Better integration between NoC network and bus structure is achieved by using addition arbiter for every pillar or vertical bus. Ciliated 3D mesh is a novel architecture that is formed by joining several layers of IP blocks while limiting the switches to a single layer or very few layers [16]. They also analyse performance of various 3D NoC architectures to highlight superior functionality of their proposed structure.

Xu et al. assess the consequence of reducing TSV count to half and quarter on 3D NoC functionality [17]. Unbalanced 3D switch distribution and varying delays for various applications are some flaws of their design. Partition islands of switches are used to create areas for allotting same TSV pad for interlayer communication that are controlled by serialization logic [18]. The average packet latency increases exponentially as the number of switches per TSV bundle rise due to serialization over TSV bundle.

3DPERM, a single cycle bufferless 3D router employs 9 permuter blocks to constitute 3-stage permutation network like CHIPPER [19]. The authors show that their design has reduced power and area overhead than a single-cycle 3D CHIPPER. Larger end-to-end latency and smaller network saturation point owing to load computation elimination are some of the key attributes of 3DPERM and 3D CHIPPER. 3DBUFFBLESS [20], is an asymmetrical 3D NoC router which is buffered in z-dimension whereas bufferless in x and y dimensions. Their proposed router merges advantages of bufferless and buffered routers to have improved routing efficiency with minimal power dissipation and area.

III. Motivation

The performance enhancements due to NoC design becomes a bottleneck with rise in number of processing cores as 2D NoC has restricted floor planning options. We perform simulations on standard 2D bufferless mesh NoC, such as CHIPPER, for various synthetic traffic patterns. Figure 1 clearly depicts rise in average latency as number of cores are varied for uniform and neighbor traffic patterns. Communication quality also diminishes as the network, which stretches across 2D plane, incurs more transmission delay and dissipates greater dynamic power.

Better routing efficiency and performance can be obtained by stacking NoC layers. 3D NoC network has decreased area footprint and better performance compared to 2D NoC designs. Agyeman et al. compares the crossbars used in 2D and 3D NoC router structures in terms of area and power consumption [21]. 3D NoC designs have higher number of interconnections, complex arbitration mechanism and employ 7-port router structure. Thus, in spite of lower packet latency in 3D NoC network, hardware overhead is more as 7-port architecture is employed for flit traversal across all three dimensions.

To improve the performance of 2D bufferless mesh NoC networks, we exploit the area and performance advantages of 2D and 3D NoC designs in our proposed design. 2 similar layers of 8x8 meshes are stacked and all routers employ 5-port CHIPPER microarchitecture. TSV based vertical interconnections formed through unused ports of edge routers are utilized for inter-layer communication.

IV. Proposed Design

The performance of any NoC network is influenced by topology, routing algorithm and router microarchitecture. We choose mesh topology for our proposed work due to its scalability, regular structure and short interconnection links. Figure 2 depicts a 128 core chip arranged as a 2D 8x16 mesh network. Figure 3 shows our proposed structure, DoLaR with 128 routers stacked into 2 layers, each of size 8x8. All the

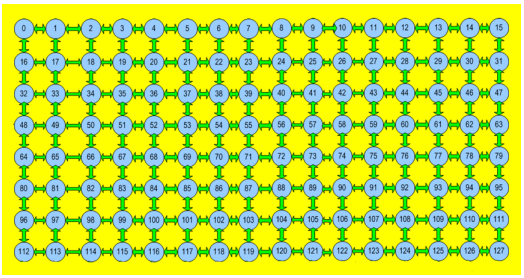

Fig. 2. 8x16 2D Mesh NoC

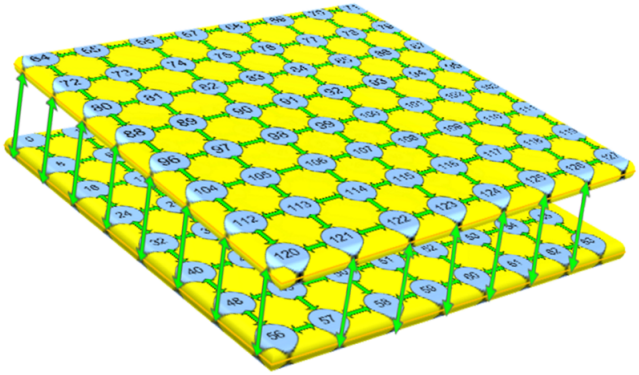

Fig. 3. DoLaR - 2 Layer 8x8 Mesh NoC

edge routers have an unused port in standard 5-port 2D mesh NoC network. We utilize these unused ports to form vertical interconnections between the layers using TSV based links.

DoLaR employs 5-port router structure of two cycle symmetrical bufferless CHIPPER, as given in figure 4. The main features of various functional units are described as follows. Input flits that progress through different modules of router pipeline are carried by four internal flit channels. Flits from nearby routers arrive at input port at the onset of each clock cycle. At the end of each clock cycle, flits get preserved in corresponding pipeline registers. Our proposed design uses Double Layer Routing algorithm, which is described in Algorithm 1. When source and destination routers are in the same layer, static XY routing is used. For inter-layer routing, flits proceed to the nearest edge router that has smallest Manhattan distance to the destination router. In bufferless routers, deadlock does not exist as cyclic dependency of resources cannot occur and the golden flit priority scheme in CHIPPER overcome livelock problem.

The incoming flits have to first pass through ejection and injection unit. A flit which is destined to local core is directed to ejection port by removing it from internal flit channel. CHIPPER supports only one ejection port and one injection port per router. Injection will happen only when any one of the internal flit channel is free since there are no buffers to

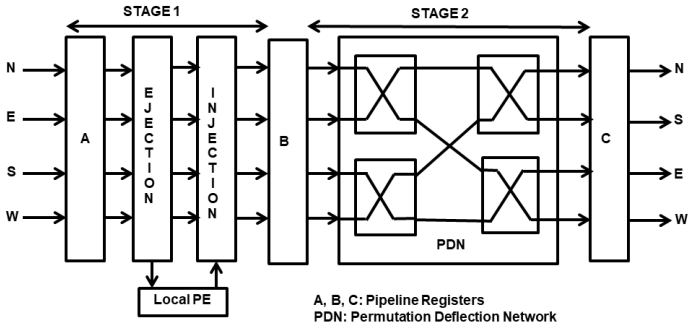

Fig. 4. Two stage router pipeline architecture of CHIPPER [5]

Algorithm 1: Double Layer Routing algorithm

Input : current_router, destination_router
Output: output port

if *(current_router_layer == destination_router_layer)* **then**
  XY routing algorithm
else
  find hops_east
  find hops_west
  find hops_north
  find hops_south
  //number of hops to destination from current router via east, west, north and south port respectively
  if *hops_east is smallest* **then**
    output port = east
  else if *hops_west is smallest* **then**
    output port = west
  else if *hops_north is smallest* **then**
    output port = north
  else
    output port = south
  end
end

store flits.

Port allocation issues arise in bufferless routers when more than one flit contend for same output port, as there are no buffers to hold the flits. Permutation network employed in CHIPPER is being used in our design. The deflected flits are redirected through freely available output links in a highly efficient parallelizable manner using golden flit concept for assigning flit priority. Highest priority will obtain productive link and rest of the flits may or may not get desired output link depending on port conflicts and extent of contention.

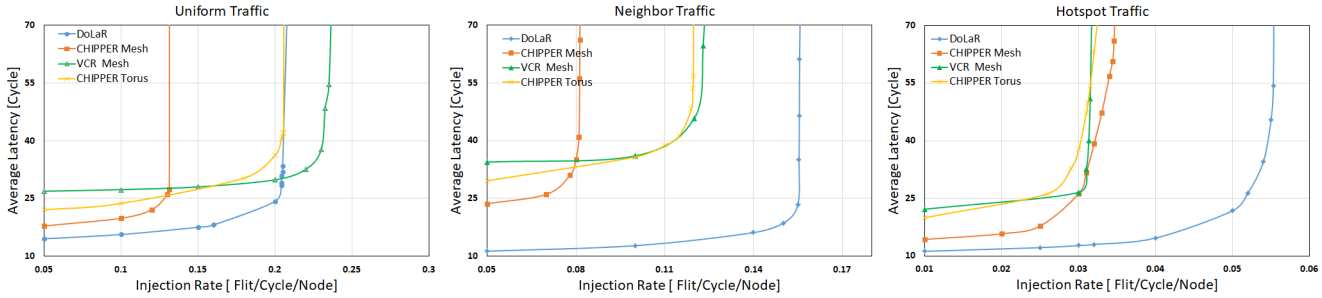

Fig. 5. Average latency comparison for different synthetic traffic patterns.

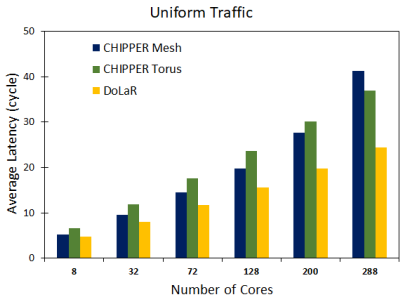

Fig. 6. Average latency versus number of processing cores

V. Experimental Methodology

We employ a cycle accurate NoC simulator Booksim 2.0 [22], that prototype traditional VC based NoC router [1]. We then make necessary alterations to model a two-cycle bufferless deflection router microarchitecture described in CHIPPER [5]. Independent routing of all the flits inside a packet is achieved by attaching header information to each and every flit, as is the typical standard followed in bufferless routers. Necessary reassembly mechanism is utilized for handling out-of-order flit delivery. To represent source and destination core address in a 128-core network, we use 14-bit header field. We employ folded torus topology for evaluation purposes to eliminate long end-around links at the expense of increasing the span of other links twofold [1]. Additional changes are made to this baseline bufferless router simulator to prototype our new design for conducting experimental analysis.

A. Synthetic Workload

We evaluate the performance of DoLaR against CHIPPER for mesh and torus topologies of 8x16 dimensions (128 nodes). Average latency, deflection rate and throughput readings are taken after adequate warm up time for different synthetic traffic patterns such as uniform, tornado, bit-complement, bit-reverse, neighbor, shuffle and hotspot by changing the injection rate from zero to saturation point.

B. Real Workloads

To show the superior performance of DoLaR, we analyse our proposed design against baseline CHIPPER employing mesh and torus topologies using real workloads such as SPEC CPU2006 benchmark application suite and PARSEC benchmark programs [23], [24]. We use Multi2Sim simulator to prototype a 128-core multicore system [25]. Each processing core is assumed to have an out-of-order x86 processing unit with 4-way set-associative, 64KB private L1 cache and 16-way set associative, 512KB shared distributed L2 cache. Each processing core is allocated with one of the SPEC CPU2006 application to run on it. Depending on misses per kilo instructions (MPKI) values found on L1 cache, we categorize benchmark applications into Low (MKPI value less than 5), Medium (MPKI value between 5 and 25) and High (MPKI value greater than 25). We produce 7 multiprogrammed workload mixes by combining various applications from benchmark suite. Multithreaded workloads are run on a similar setup with slight alterations to produce adequate traffic for analysis purpose. To simulate network operations, NoC simulator is fed with network traffic produced by running the real workloads.

VI. Results and Analysis

We compare the performance of DoLaR against conventional mesh topology based VCR and standard CHIPPER for mesh and torus topologies. For our analysis, we assume 16 VCs per input port for VC router. We use deterministic and deadlock free XY routing algorithm for VCR, CHIPPER mesh and torus designs to evaluate performance enhancement of our proposed approach.

A. Effect on Average Flit Latency

Flit latency is defined as the total time elapsed between flit creation time at source node and flit arrival time at destination node, including queuing time at source core. Figure 5 shows average flit latency comparison between 8x16 2D mesh VCR, 8x16 2D mesh CHIPPER, 8x16 torus CHIPPER and our proposed design for various synthetic traffic patterns. DoLaR reduces average flit latency by 21%, 14% and 21% for uniform, bitcomp and hotspot traffic respectively, compared to CHIPPER mesh. There is exponential rise in average latency value as injection rate approaches saturation. Lower and broader flit latency curve shows better router performance. VCR saturate early as static XY routing used makes it congestion prone. DoLaR is a better option for high network injection rate applications as it has lower latency value

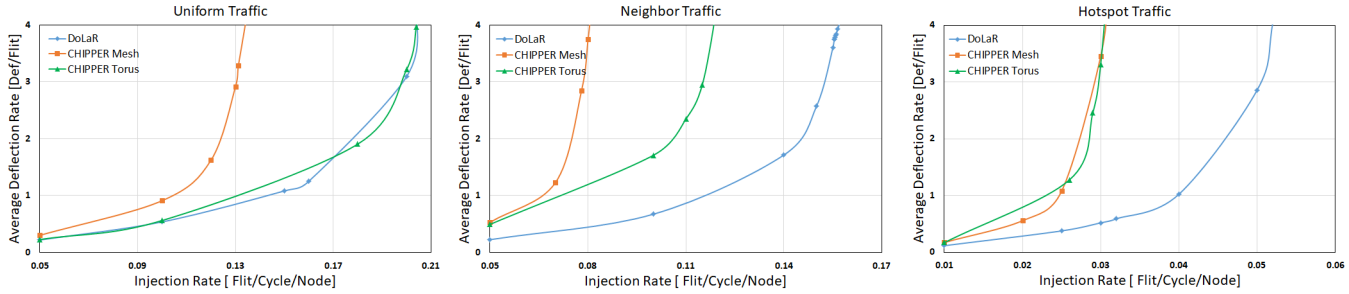

Fig. 7. Average flit deflection rate comparison for different synthetic traffic patterns.

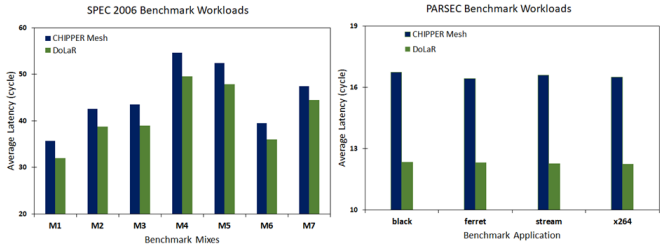

Fig. 8. Average latency for real applications

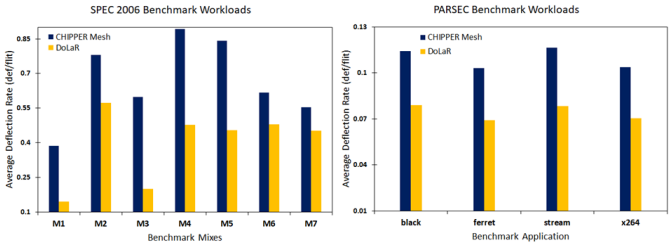

Fig. 9. Average deflection rate for real applications

and also extends network saturation point compared to other designs under consideration.

Figure 6 shows how average latency values get affected with scaling of number of processing cores. When compared with CHIPPER mesh and torus designs, DoLaR design has significant drop in average latency values as number of processing cores is increased. Figure 8 depicts notable reduction in average flit latency compared to mesh topology based CHIPPER for multiprogrammed and multithreaded workloads.

B. Effect on Average Deflection Rate

Deflection rate is calculated as average number of deflections occurring per injected flit. As injection rate rises, due to more port contentions, deflection rate will also increase. Figure 7 and figure 9 clearly depict superior performance of our design for synthetic and real traffic respectively. The reduction in deflection rate indicates decreased network activity thereby improving dynamic power savings across links.

C. Area Overhead

The total area overhead in a NoC network includes router overhead and wiring overhead. Router overhead comprises of

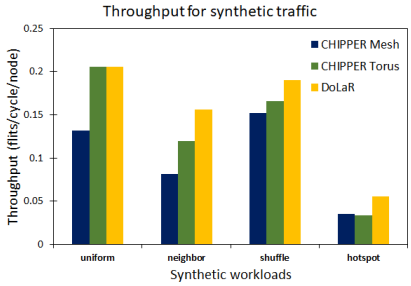

Fig. 10. Througput comparison for different synthetic traffic patterns.

overall router area which is based on total number of routers in NoC and per router area overhead that depends on number of ports in each router. 5-port router architecture is generally utilized in 2D NoC whereas 7-port structure is employed in standard 3D NoC designs. As DoLaR design and standard CHIPPER design uses the same 5-port router architecture, their router area overhead remains almost comparable. The negligible router area overhead due to the modified routing logic employed in DoLaR is inconsequential compared to significant gains achieved in terms of average latency and deflection rate reductions.

Wiring overhead for 2D NoC network is only due to horizontal wirings. Thus, 2D mesh of dimension 8x16 requires 232 horizontal links. 3D NoC incurs overhead due to inter-layer via footprint in addition to wiring overhead caused by horizontal and vertical links. DoLaR employs 224 horizontal links, which is twice that of 8x8 mesh NoC and extra vertical links (28 TSV links) for interconnecting the edge routers. Though TSV links incurs some metal and silicon area, DoLaR has minimal footprint as two layers of 8x8 mesh are placed one above the other.

D. Effect on Throughput

Throughput is defined as the amount of flits ejected from network per router per cycle. Number of physical links and average hop count determine improvement in throughput for multi-layer networks. Figure 10 depicts throughput comparison between DoLaR, CHIPPER mesh and torus designs for various synthetic traffic patterns. DoLaR has better throughput showing greater amount of sustainable traffic owing to its reduced average hop count and more number of physical links.

E. Effect on Router Pipeline Delay

Router delay is defined as the time taken by a flit to travel from input port to output port of a router. To calculate router pipeline latency, we implement and synthesize Verilog HDL models of router employed in CHIPPER and DoLaR using Xilinx Vivado Design Suite-HLx. As both CHIPPER and DoLaR have 5-port deflection router structure, they employ similar functional units, except for the routing logic. Since the second stage of CHIPPER has more delay than its first stage, router pipeline frequency of CHIPPER is determined by the delay of its second stage. So, pipeline frequency of DoLaR will be same as that of CHIPPER.

F. Effect on Dynamic Power Consumption across NoC links

Power dissipation across individual routers and inter-router wire links collectively determine total NoC network power. The underlying interconnection architecture decides the networks reliability in terms of power dissipation. Power consumption in network is proportional to packet injection rate as it decides the amount of network activity. The power dissipation across the router is same in DoLaR and 8x16 CHIPPER as both of them employ similar functional units in their router architecture.

The area and power associated with the network is studied and compared using Orion [26]. The standard 65nm technology at 1GHz operational frequency with one cycle inter-router link delay is presumed for our analysis. For both CHIPPER and DoLaR, router area remains comparable as the same 5-port router structure is followed. DoLaR reduces dynamic power dissipation across NoC links by 32% for uniform traffic, 29% for bit-complement and 37% for hotspot traffic when compared with CHIPPER mesh design. The reduced average hop count and deflection rate of our proposed design is instrumental in reducing the dynamic power across NoC links.

VII. Conclusion

The emergence of NoC as a preferred communication framework has repressed design issues like bottleneck challenges and scalability problems encountered by traditional SoC based architectures. DoLaR is proposed in this paper, where two identical layers of 8x8 meshes are stacked one above the other using minimal number of vertical interconnections along the edge routers. Area and performance benefits of 2D and 3D architectures are put to use in our design approach with minimum TSV based vertical connections and utilizing standard 5-port bufferless router architecture. Experimental outcomes indicate that DoLaR achieves better network performance when compared with 2D CHIPPER mesh and torus designs.

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