# Scalable On-chip Interconnects For Many-Core Systems

**May 24 - 30, 2017 @ Indian Institute of Technology Guwahati, Assam.**

## Course Overview & Objective

Power and thermal constraints has led the processor industry to embrace multicore architectures. In continuation with the evolution of processor technology, researchers have started focusing on many core processor designs with more than 100 cores on a single chip. This paradigm shift towards many core designs has resulted in a renewed interest in on-chip interconnect design due to the complexity and criticality involved in the communication pattern of such massively parallel systems. On-chip interconnects play a major role in shaping the power and performance profiles of multicore processors. As a scalable substitute for time shared on-chip bus, Network-on-Chip (NoC) is proposed as the communication infrastructure in modern multi/many-core System-on-Chips (SoC). Efficient communication in NoC is critical to the overall SoC performance.

This GIAN course is basically organized into 4 modules: (1) Introduction to NoC architectures, (2) Performance improvement in NoC by adaptive routing and throttling, (3) Energy efficient NoC designs, (4) Emerging NoC architectures. The course contains (a) regular lecture sessions (b) hands on sessions on open source full system architectural simulator-GEM5, together with interconnect model GARNET (c) problem solving & tutorial sessions for deeper understanding of advanced concepts. The course also provides an opportunity to the participants who are interested in the field of computer architecture in general and on-chip interconnection systems in particular to have fruitful association/ collaboration with Multicore Architecture and Systems (MARS) Research Group of CSE department, IIT Guwahati in terms of collaborative research, student project co-mentoring and internships. The course will also throws light on few emerging research problems in NoC domain upon which the participants can work on, once they go back to their parent institutions with necessary support from the course coordinator.

# Detailed Course Plan

| Day | Session | Time | Topic |
|---|---|---|---|
| 24 May 2017<br>Wednesday | | 10:00 am - 11:00 am | Inauguration function.<br>Introduction and overview of the course |
| | Lecture 1 | 11:30 am - 1:00 pm | Emerging VLSI trends and multicore chips, paradigm shift from time shared bus to packet based interconnection network. Introduction to NoC system. |
| 25 May 2017<br>Thursday | Lecture 2 | 9:30 am - 11:00 am | Building blocks of an NoC system- topology, routing, flow control, switching and router microarchitecture |
| | Lecture 3 | 11:30 am - 1:00 pm | Routing algorithms, adaptive routing algorithms in NoCs, input/ output channel selection strategies, load balancing and link utilization techniques |
| | Tutorial-1 | 2:30 pm - 4:30 pm | Numerical problem solving session on fundamental topics covered in lectures 1, 2 and 3. |
| 26 May 2017<br>Friday | Lecture 4 | 9:30 am - 11:00 am | Application specific routing algorithms, adaptive routing by exploiting memory level parallelism, adaptive flow control by advanced throttling mechanisms. |
| | Lecture 5 | 11:30 am - 1:00 pm | Buffer less and minimally buffered NoC router designs, techniques for controlling aging of NoC links |
| | Practice Session | 2:30 pm - 4:30pm | Hands on session on GEM5 + GARNET simulator |
| 27, 28 May 2017<br>Saturday, Sunday | **Off Day**<br>Hands on session on GEM5 + GARNET simulators (for interested participants) | | |
| 29 May 2017<br>Monday | Lecture 6 | 9:30 am - 11:00 am | Performance improvement in TCMPs at NoC level, data encoding techniques in NoC, fault tolerant NoC designs. |
| | Lecture 7 | 11:30 am - 1:00 pm | Emerging trends in NoC architectures- 3D NoCs, wireless NoCs, optical NoCs, Fault tolerant NoCs, |
| | Tutorial 2 | 2:30 pm - 4:30 pm | Numerical problem solving session on topics covered in lectures 4, 5, 6 and 7. |

| | | | |
|---|---|---|---|
| 30 May 2017 Tuesday | Lecture 8 | 9:30 am to 11:30 am | Discussion on emerging research problems and action plan/ road map for follow up activities |
| | Exam | 2:00 pm to 4:00pm | Course Assessment Test (optional) for participants who need grade card of the course |

## Who can attend?

- Faculty from academic and technical institutions.
- Persons from R&D organizations/ industries and staff working in R&D projects.
- Student from CSE/ECE/IT background (B.Tech/MSc/MCA/M.Tech/Ph.D).

## What is the course fee structure?

The participation fees for taking the course is as follows:

- **Participants from abroad : US$ 500**
- **Industry/ Research Organizations : INR 8000**
- **Faculty from Academic Institutions: INR 4000**
- **Indian students : INR 1000 (*Refundable after course completion).**

The above fee includes all instructional materials, computer use for lab/ tutorial sessions and internet facility. The participants will be provided with twin sharing accommodation on payment basis at IITG guest house/ student hostels.

## What is the registration procedure?

1. Go to GIAN website (http://www.gian.iitkgp.ac.in/GREGN/index) and register. You need to pay a one-time fee of INR 500 /- for registration.
2. Select the course – **161006D01: Scalable On-chip Interconnects for Many-Core Systems**
3. Once you enroll for the course, the course coordinators will be notified. The course coordinator will shortlist the candidates, and selected candidates will be notified by email.
4. The selected candidates must pay the applicable fees by a demand draft taken in favor of **REGISTRAR, INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI** payable at **GUWAHATI.**
5. Fill the course registration form in the GIAN portal. Send the print out of the course registration form and the Demand Draft to the course coordinator (postal address given below) within stipulated time mentioned in the selection mail.
6. Please keep the copy of the registration form and DD for future reference and correspondence.
7. Inform the course coordinator if you need campus accommodation ( self-payment basis)

## Resource Persons

### (1) Dr. Maurizio Palesi **Profile Link - http://utenti.dieei.unict.it/users/mpalesi/**

He is a pioneer researcher in the field of on-chip interconnects. Currently he is an associate professor in Department of Electrical, Electronics and Computer Engineering, University of Catania, Italy. His general research area is embedded systems design with special focus to instruction level power modelling, multi-objective optimization, design space exploration of parameterized SoC platforms, low-power design and Network on Chip (NoC) architectures. He has co-authored over 40 high impact journal papers and over 60 peer reviewed conference proceedings papers. He is an editorial board member of many system level journals and serves as technical program committee member for many premier computer architecture conferences. He is associated with the NoCArc workshop (http://nocarc.unikore.it/index.html) since its inception as general chair and steering committee member. He is a member of the European Network of Excellence on High-Performance Embedded Architecture and Compilation (HiPEAC).

### (2) Dr. John Jose **Profile Link - http://www.iitg.ernet.in/johnjose/**

He is as an assistant professor in department of Computer Science & Engineering, Indian Institute of Technology Guwahati, Assam. His research interests are in computer architecture with a special focus to performance optimization related to on-chip memory and communication aspects of many core processors. He has published over 15 research papers in the broader domain of congestion management techniques in adaptive NoC routers, energy efficient NoC router designs, and fault tolerant NoC designs at premier conferences like ICCAD, DATE, ICCD, VLSI-SoC, GLSVLSI, VLSID and NoCArc. He is a reviewer for many national / international peer reviewed journals and member of technical program committee for many IEEE/ACM national and international conferences. He is a resource person to many computer architecture related symposia and workshops. Currently he is guiding four doctoral and five master thesis in the area of multicore interconnection systems. He is the principal investigator of two sponsored R&D projects funded by DST.

## Course Coordinator

**Dr. John Jose, Assistant Professor,**
**Multicore Architecture and Systems (MARS) Lab,**
**Department of Computer Science and Engineering,**
**Indian Institute of Technology Guwahati,**
**North Guwahati, Assam, Pin 781039.**
**Phone - Office : 0361-2583256, Mobile : +91-9048665842 E-mail :johnjose@iitg.ernet.in**