Registration

Name of the Applicant (first, last):
……
……
Gender: …….. ……..…
Designation: ……...

Affix passport size photograph

Highest Qualification: ……
Name and Address of the Organization/Institute:……
……..
Category : (GEN/OBC/SC/ST/Others)……
City/town:……..……..
Email:……..
Phone Number:……..
Mobile Number:……..
Do you need accommodation?
(Yes/No):……..
Transaction ID (Applicable for Online Transaction):……
Signature of the Applicant:……...
Signature and Seal of the Forwarding Authority
Name .....
Designation .....

Note: The Faculty/Staff are requested to submit the NOC from respective department before attending the session.

Registration Fee

Registration Fee (Including Course Material, Snacks and Lunch)

Rs. 2,500/- for Faculty, Lab Technicians and Project Staff **Rs. 5,000/-** for Industry Personnel, Research Scholars and Students.

Mode of Payment: Online Only (RTGS/NEFT)

For Online Transfer

Bank Name: State Bank of India
Account Name: IIT Guwahati R&D E&ICT Academy
Account No.: 36071160089
IFSC Code: SBIN0014262
Bank Name: State Bank of India
Bank Address: IIT Guwahati, GHY- 39.

Course Coordinators from Academy

- **Dr. Gaurav Trivedi**
  Co-Principal Investigator
  E&ICT Academy, IIT Guwahati
- ***Dr. John Jose***
  Assistant Professor,
  CSE Department, IIT Guwahati

Expert from Industry

- ***Mr. H.Balachander***
  FAE Manager CoreEl Technologies
- **SCL Chandigarh**

Course Programme

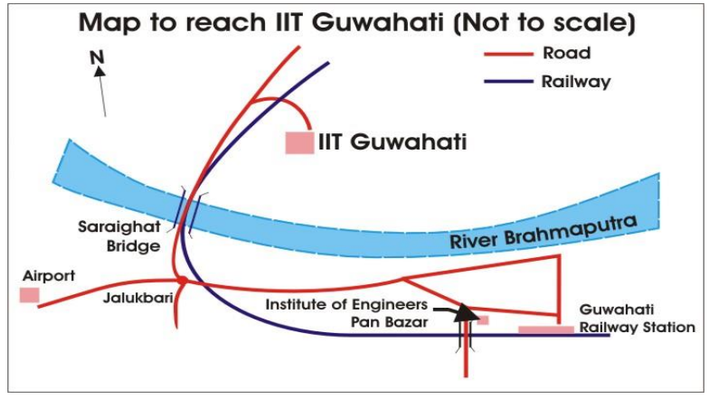
Faculty Development Programme is Split into three parts:

- Lectures.
- Labs/Hands-on sessions daily.
- Assignment and Project.

Contact Details

For more details or any queries please contact
Project Manager
E&ICT Academy IIT Guwahati
Email: eictacad@iitg.ernet.in, eictacad@gmail.com
Phone No: +91-3612586442

How To Reach IIT Guwahati



सत्यमेव जयते

An Initiative of Department of Electronics & Information Technology (DeitY), Ministry of Communications and IT, Government of India

Electronics & ICT Academy
IIT Guwahati, Assam

CoreEL Technologies
Enabling Excellence

A Faculty Development Programme on

Digital VLSI

support from Coreel Technologies.
In Association with SCL Chandigarh

Applications are invited from Faculty Members/ Research Scholars/PG & UG Students/Lab Technicians/Project Staffs from Universities/Colleges/Schools & Industry Personnel working in the concerned discipline can attend the Faculty Development Programme on

"Digital VLSI "

Course Date: 28 April-12 May 2017
Last Date of Registration: 20.04.2017
(Online Registration Link will be open from 01.04.2017)
Venue: IIT Guwahati

Course Outcome

The participants are expected to understand:

- Understand the Vivado design flow
- Create and debug HDL designs
- Configure FPGA architecture features, such as Clock Manager, using the Architecture Wizard
- Communicate design timing objectives through the use of Xilinx Design Constraints
- Pinpoint design bottlenecks using the reports
- Utilize synthesis options to improve performance
- Create and integrate IP cores into design flow using IP Catalog
- Use Logic Analyzer to perform on-chip verification
- Perform simulation verifcation
- Apply directives to optimize design performance
- Perform system-level integration of blocks generated by the VivadoHLS tool
- Rapidly architect an embedded system targeting the ARM processor of
- Zynq located on ZedBoard using Vivado and IP Integrator
- Extend the hardware system with Xilinx provided peripherals
- Create a custom peripheral and add it to the system
- Write a software application to access peripherals
- Perform IP-level Bus Functional simulation verification

Assignments and Project

Assignments will be of the following type:

- MCQ based questionnaire.
- Programming Assignments (Problem statement will be provided.)

At the end of the course “Project” will be assigned to the participants which would be an application development demonstration of the tools usage.

Preferred Pre- Requisites for the Course

The preferred Pre-Requisites for the course are:

- Basic Digital Concepts.
- Basic knowledge on Xilinx FPGA
- Basic Knowledge on Verilog/VHDL.
- Familiarity with Windows & Linux Environment.

Hands-on Session

The Hands- on session will include the following:

- **Hands-on using SCL PDK Digital Design significance to signoff**
- Vivado Design Flow (Synthesizing a RTL Design
- Implementing the Design Using the IP Catalog and IP Integrator
- Xilinx Design Constraints
- Simple Hardware Design using MMCM
- Hardware design using PLL
- FSM design
- Simple Hardware Design using block memory
- Designing FIFO
- Creating simple UART
- Simple pattern detector using FSM
- Testbenches features & Vivado simulation features Creating simple UART
- Implemeting pattern detector in hardware and debugging using vivado logic analyzer
- Teraterm/hyperterminal based testing with vivado logic analyzer
- Creating Project and Understanding Reports
- Optimizing Performance through Pipelining
- Improving Area and Resource Utilization
- Designing an Audio System
- Simple Hardware Design
- Adding Peripherals in Programmable Logic
- Creating and Adding Your Own Custom IP

About E&ICT Academy

Electronics and ICT Academy is an initiative of Department of Electronics & Information Technology (DeitY) Ministry of India for Faculty/ Programme. Academy has planned short term training programmes on fundamental and advanced topics in IT, Electronics & Communication, Product Design, Manufacturing with hands on training and project work using latest software tools and systems.

In addition, the Academy will conduct specialized/customized training programmes and research promotion workshops for corporate sector & educational institutions.

Objective of the Course

Course Objective is to provide basic knowledge in Digital VLSI using FPGA board. The programme will focus on practical aspects and include examples which are relevant to the current industry requirements.

Lab sessions will include the following:

- **Digital Design concepts using SCL PDK cases with Hands-on.**
- FPGA design flow using Vivado.
- Clocking resources implementation in Vivado & Static timing analysisVectorization.
- Block Memory implementation in vivado.
- FSM implementation in Vivado & XSIM simulation
- Vivado logic analyzer & its features
- Introduction to HLS
- Optimizing for Area and Resources

Who Can Attend

Programme is open to Faculty Members, Research Scholars, PG & UG Students, Lab Technicians and Project Staffs from Universities , Colleges & Schools. Industry Personnel working in the concerned/allied discipline may also apply.

How to Apply

Online – The participants may log on to the E&ICT Academy, IIT Guwahati website: http://eictacad@iitg.ernet.in and fill up the google doc application form.

Through Email – Scanned copy of the filled in application form duly endorsed by the, forwarding authority is to be mailed at E&ICT Academy’s email id (eictacad@gmail.com, eictacad@iitg.ernet.in).

Application format given in this brochure may also be downloaded from the website.

Contact Hours for the Course
90 Hrs (Theory, Hands-on & Tutorial)

For details please log on to Electronics and ICT Academy website: http://eict.iitg.ernet.in/