NoCArc 2022

https://www.nocarc.org/

15th International Workshop on Network on Chip Architectures
October 5 , 2022

To be held in conjunction with the 55th Annual IEEE/ACM International Symposium on Microarchitecture®
Chicago, Illinois, USA

NoCArc 2022

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The accepted conference papers will be invited for an extended journal version, to be published in a special issue TBD.

General Information

Networks-on-Chip (NoCs) play a crucial role in determining the overall performance, energy usage, and reliability of many-core processing architectures. NoCs are part of an increasingly large number of products that we use every day – demonstrating that the NoC paradigm is practical, scalable, and can be adapted to support multiple computational paradigms, ranging from multiprocessing and reconfigurable computing to the emerging areas of AI and neuromorphic computing. The goal of the NoCArc Workshop is to provide a forum for researchers and practitioners to present and discuss innovative ideas and solutions related to the design, implementation, testing and application of NoCs and NoC based many-core architectures.

Areas of Interest

The workshop will focus on issues related to the design, analysis, testing, and application of on-chip networks. The topics of specific interest for the workshop include, but are not limited to:

Machine Learning (ML) and NoC-based systems
- ML for modeling and prediction
- ML based algorithms, optimization, and design methodologies
- Novel interconnections for domain specific ML architectures
- Memory access for the NoC-based ML systems

NoC Architecture and Implementation
- Topologies, routing, and flow control
- Managing QoS
- Reliability issues
- Security issues
- Design methodologies and tools

NoC Analysis, Optimization, and Verification
- Power, energy, and thermal issues
- Benchmarking and experience with NoC-based systems
- Modeling, simulation, and synthesis
- Verification, debug, and test of NoCs and NoC-based systems
- Metrics and benchmarks

NoC Applications
- Mapping of applications onto NoCs
- Real and industrial NoC case studies
- NoCs for FPGAs, structured ASICs, CMPs, and MPSoCs
- NoC designs for heterogeneous systems

NoC at System-level
- Design of memory subsystem
- NoC support for memory and cache access
- OS support for NoCs
- Programming models including shared memory, message passing, and novel programming models
- Large-scale systems (datacenters and supercomputers) with NoC-based systems as building blocks
- NoCs and datacenters

Emerging NoC Technologies
- Wireless, Optical, and RF
- NoCs for 3D and 2.5D packages
- Approximate computing for NoCs and NoC-based systems
- Chip-to-Chip Interconnects

Submission Guidelines

Besides regular papers, papers describing "work in progress" or incomplete but sound new innovative ideas related to the workshop theme are also encouraged. Please, visit the workshop webpage (https://www.nocarc.org/) for additional information about the submission process.

Important Dates

Abstract submission deadline:	**July 15, 2022**
Full paper submission deadline:	**July 22, 2022**
Author notification:	**August 12, 2022**
Camera-ready version due:	**August 19, 2022**
NoCArc Workshop:	**October 5, 2022**