Mid Semester Examination: CS-421 (Computer peripheral and Interfaces)

Deptt. of Computer Science & Engg. , IIT Guwahati

Full Marks: 50, Duration: 2 Hours, Timing 10.00AM-12.00Noon, Date: 20th Sept 2010

1. [10] Answers the following short questions:
   a. [2] What is memory mapped I/O and IO mapped IO. Explain data movements (instruction and addressing) from IO to CPU and addressing methods in both the cases?
   b. [3] What are different conditions to satisfy for data transfer form CPU to I/O or vice versa? What is difference between Status check, Polling and interrupt?
   c. [2] Explain steps in transferring data from Memory to IO using DMA controller using HOLD & HLODA.
   d. [3] What algorithms/methodologies are used for Analog to Digital conversion? What are different performance characteristics measures of DAC?

2. [10] Suppose a graphics display having resolution 1600x1200 (1.9MegaPixel) with Frame buffer containing YUV values instead of RGB color values. **The human eye has fairly little color sensitivity**: the accuracy of the brightness information of the luminance channel (Y) has far more impact on the image discerned than that of the other two (U and V). In case of RGB we store 24 (8+8+8) bits per pixel in frame buffer , but in YUV case we store 4x8+8+8=48 bits for group of 4 pixels (that is 4 Y values 8 bit each + 1 U value of 8 bit + 1 V value of 8 bit for group of 4 adjacent pixels). The RGB values can be computed from YUG values by a decoder to render the screen. (Assume YUG to RGB decoder is a black box, you don't require to draw the internal and you can use 4 such decoder).

   Design a circuit block diagram to refresh the above designed graphics screen at **30frame/S**. What should be Clock values for the both row and column counter to perform at this rate? What should be maximum delay of such YUV to RGB decoder?

3. [10] Design a real time clock with hours, minute and second with 6 seven segment LED display. Interface an **8254 PIT** and a group of 6 seven segment LEDS using an **8255 PPC** to 8085 microprocessor. Generate 1 Second clock pulse using two counter (ctr0 & ctr1) of 8254PIT and one counter (12hr.60min.60Sec=43200 < max of 16 bit number 65368) for real time clock (ctr2). After every 1 second (generate interrupt to read) read the RTC counter value and format the value in proper format (BCDs HH:MM:SS) and send to output port using 8255.

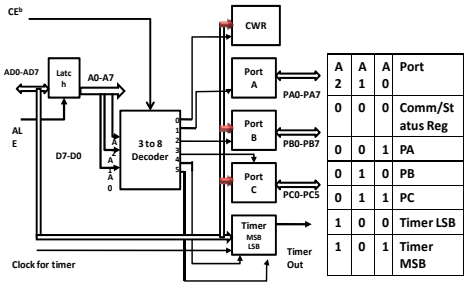
   Draw the interface diagram and write interfacing (8085 assembly) program to perform this work.

4. [10] Design interface and write interface program to interface seven I/Os devices namely Emergency actions, A/D converter, Heater, Keyboard, Display, Special money transaction device and printer using **8259** interrupt controller. Design interface the circuit to work at address 80H for ICW1 and 81H for ICW2. Special money transaction device have lower priority then Emergency actions. You have to ensure that Special money transaction device should not be interrupted once its ISR started till the end of its ISR using mask bit. Assume interrupt vector address for each interrupts and use properly in your interface program.

   Determine the values of ICWs, OCWs in this case for your interface structure. Draw the interface diagram and write interfacing (8085 assembly) program (to initialize ICWs & OCWs) to perform this work.

5. [10] Interface a LCD monitor via RS-232 port using a 8251 USART controller. Design the interface diagram so that you should be able to address the SUART at 5EH and 5FH for data and control respectively. Specify initialization instructions and status word to transmit characters with Async mode with 9600 baud rate, 8 bit character length, 2 stop bits and without any parity check.

   Write instructions to initialize USART and read status word and setup a loop until the USART transmitter is ready. Using this write an interface program that will send 10 characters from memory to LCD monitor for display.



A2	A1	A0	Port
0	0	0	Comm/Status Reg
0	0	1	PA
0	1	0	PB
0	1	1	PC
1	0	0	Timer LSB
1	0	1	Timer MSB

8155 IO/Timer

MSB							
M2	M1	T13	T12	T11	T10	T9	T8
LSB							
T7	T6	T5	T4	T3	T2	T1	T0

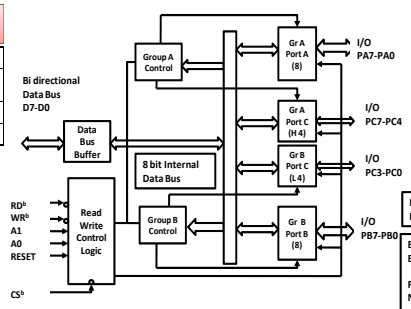
- M2, M1: mode bits:
  - 00: Single square wave of wavelength TC/2 (TC/2,TC/2 if TC even; [TC+1/2],[TC-1/2] if TC odd)
  - 01: Square waves of wavelength TC (TC/2,TC/2 if TC even; [TC+1/2],[TC-1/2] if TC odd)
  - 10: Single pulse *on* the TC'th clock pulse
  - 11: Single pulse *on* every TC'th clock pulse.

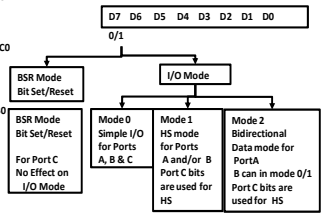
D7	D6	D5	D4	D3	D2	D1	D0
Timer Command		IEB	IEA	PC		PB	PA

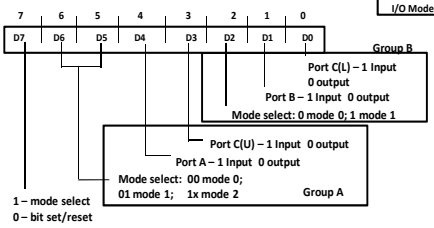
- D0, D1: mode for PA and PB, 0=IN, 1=OUT
- D2, D3: mode for PC
- D4, D5: interrupt EN for PA and PB, 0=disable 1=enable
- D6, D7: Timer command:
  - 00: No effect
  - 01: Stop if running else no effect
  - 10: Stop after terminal count (TC) if running, else no effect
  - 11: Start if not running, reload at TC if running.
- Port C bits (D2, D3)

ALT	D3	D2	PC5	PC4	PC3	PC2	PC1	PC0
1	0	0	IN	IN	IN	IN	IN	IN
2	0	1	OUT	OUT	OUT	OUT	OUT	OUT
3	1	0	OUT	OUT	OUT	STB_A	BF_A	$INTR_A$
4	1	1	STB_B	BF_B	$INTR_B$	STB_A	BF_A	$INTR_A$

8255 PPC

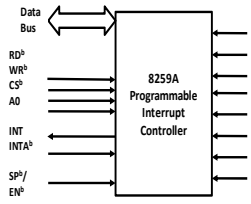


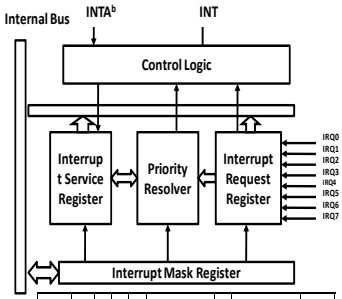




CS^b	A1	A0	Sel
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	CRW

8259 PIC





CS	A0	Initialization	OCW
0	0	ICW1	OCW1
0	1	ICW2 ICW3,ICW4	OCW2,OCW3, OCW4
1	X	Not Address	Not Address

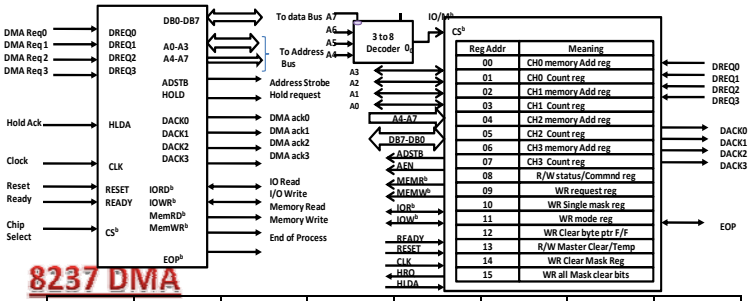
AD0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	LTIM	0	SGNL	IC4
		0 for x86			0/1 Edge /Level Trigger		1=single 0=Cascade	

AD0	D7	D6	D5	D4	D3	D2	D1	D0
1	M7	M6	M5	M4	M3	M2	M1	M0
	Interrupt Masks: 1= Mask Set, 0 =Mask reset							

AD0	D7	D6	D5	D4	D3	D2	D1	D0
1	T7	T6	T5	T4	T3	T2	T1	T0
	T7=T0 is the assign to IR0, Vector address for ISR							

AD0	D7	D6	D5	D4	D3	D2	D1	D0
0	R	SL	EOI	0	0	L2	L1	L0
	Rotate	Specific	EOI			IR Level to be acted Upon (0-7)		

8237 DMA



Reg Addr	Meaning
00	CH0 memory Add reg
01	CH0 Count reg
02	CH1 memory Add reg
03	CH1 Count reg
04	CH2 memory Add reg
05	CH2 Count reg
06	CH3 memory Add reg
07	CH3 Count reg
08	R/W status/Commnd reg
09	WR request reg
10	WR Single mask reg
11	WR mode reg
12	WR Clear byte ptr F/F
13	R/W Master Clear/Temp
14	WR Clear Mask Reg
15	WR all Mask clear bits

CMD

D7	D6	D5	D4	D3	D2	D1	D0
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
DACK Sense Active Low/High	DREQ Sense Active Low/High	Late/Extended Write Selection	Fixed/ Rotating Priority	Normal/ Compressed Timing	Enable/Disable Controller	Dis/En CH0 Address Hold	Dis/En Mem-mem Transfer

Mode

D7	D6	D5	D4	D3	D2	D1	D0
00=Demand, 01=Single 10=Bloc, 11=Cascade		INC/DEC Address	Dis/Ena Auto Initialisation	00=verify Transfer 01=Write , 10=Read transfer		Channel Select 00=CH0, 01=CH1, 10=CH2, 11=CH3	

Req

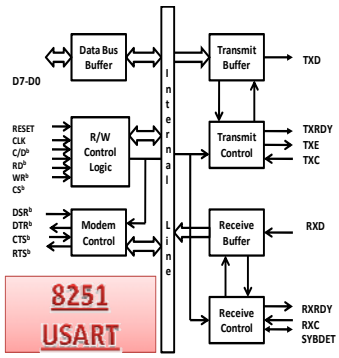
D7	D6	D5	D4	D3	D2	D1	D0
XXXXX Don't Care				Reset/Set REQ bit	00-11 Channel Select 00=CH0, 01=CH1, 10=CH2, 11= CH3		

D7	D6	D5	D4	D3	D2	D1	D0
XXXX Don't Care				0/1	0/1	0/1	0/1
				CH3 Mask Bit	CH2 Mask Bit	CH2 Mask Bit	CH0 Mask Bit

Status

D7	D6	D5	D4	D3	D2	D1	D0
0/1, CH3	0/1,CH2	0/1, CH1	0/1, CH0	0/1, CH3	0/1, CH2	0/1, CH1	0/1, CH0
CH# Request				CH# Has reached TC			

8251 USART



CS^b	C/D^b	RD^b	WR^b	Meaning
1	X	X	X	Data Bus Tri-state
0	X	1	1	Data Bus Tri-state
0	1	0	1	Status → CPU
0	1	1	0	Control Word← CPU
0	0	0	1	DataBuff → CPU
0	0	1	0	DataBuff ← CPU

EH	IR	RTS	ER	SBRK	RxE	DTR	TxE

TxE: transmit enable (0/1 Enable Disable)
DTR: data terminal ready (1=ENABLE DTR)
RxE: receiver enable (1/0=EN/DISABLE)
SBPRK: send break character 1= force TxD low
ER: error reset (Reset Flags: Parity ,Over run, Framing Error of Status Word)
RTS: request to send (1= Enable Request to send)
IR: internal reset (Reset 8251 to mode)
EH: enter hunt mode (1=search for Sync Character)

D7	D6	D5	D4	D3	D2	D1	D0

Framing Control # of Stop bits
00: invalid
01: 1 bit
10: 1.5 bits
11: 2 bits

Parity Control
X0=No Parity
01: Even
11: Odd

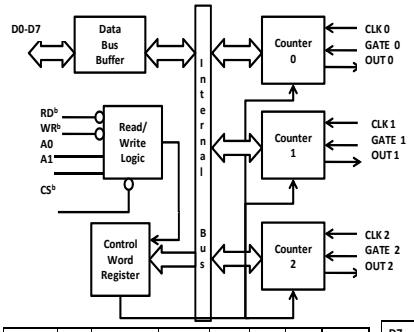
Character length
00: 5 bits
01: 6 bits
10: 7 bits
11: 8 bits

Baud Rate
00: Syn. Mode
01: x1 clock
10: x16 clock
11: x64 clock

DSR	SYN DET	FE	OE	PE	Tx EMPTY	RxRDY	TxRDY

TxRDY: transmit ready (DB Buffer is empty)
RxRDY: receiver ready
TxEMPTY: transmitter empty
PE: parity error (1=when PE detected)
OE: overrun error
FE: framing error (Aynsc only, Valid stop bit not detected)
SYNDET: sync. character detected
DSR: data set ready (DSR set at 0 level)

8254 PIT



- Mode 0 : Interrupt on Terminal count
- Mode 1 : Hardware Retriggerable One Shot
- Mode 2 : Rate Generator
- Mode 3 : Square wave generator
- Mode 4 : Software Triggered Strobe
- Mode 5 : Hardware Triggered Strobe

A1	A0	Selection
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Register

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC2	RW1	RW0	M2	M1	M0	BCD
Select Counter 00: Counter 0 01: Counter 1 10: Counter 2 11: Read-Back Command		Read Write 00: Counter latch Command 01:RW LSByte only 10: RW MSByte only 11:RW LSByte first then Msbyte		000 : Mode 0 001 :Mode 1 X10 :Mode 2 X11 :Mode 3 100 :Mode 4 101 : Mode 5			0/1 = Binary / BCD Mode

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC2	$COUNT^b$	$STATUS^b$	CNT 2	CNT 1	CNT 0	0
11: Read-Back CMD		If (D5=0) count is lateched		D3=1 select CTR 2 D2=1 select CTR 1 D1=1 select CTR 0			