CS224 : Assignment 5

Date of Demonstration 25th April 2023, Lab Timing (2PM-5PM), 26% (18+6) weight

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Part I: Design of DRAM Memory using HDL and demonstration using Simulation

Design and implement DRAM with 2 channels, 8 ranks per channel, 16 Banks per rank, and each bank of size 256 rows and 1024 columns. Assume the cache block size is 64B. Assume the processor-generated address is 32-bit in size and the physical/memory address is 26-bits, (we can ignore MSB 6-bit of 32-bit address). You do not need the store actual data to be placed in the DRAM but simulate the DRAM structure. The abstract view of the memory is shown in Figure A.

Your design should support

- Page Mode Access for each bank. Accessing a block (read/write) from Buffered Page takes 32 cycles but reading a page from the row to the page buffer takes 128 cycles, and writing the page buffer to a row of the bank takes 256 cycles.
- Optional: Every 5000 cycles interval, all the un-accessed rows of the bank need to refresh the data
- Every channel has a block access status register and it can store, information about 8 block accesses. The information can be read, write, served, and ready to serve.
- Processor (or from L2) can send further a request if all its dependent requests are served.

Assume the processor is connected to the memory with 64 bits of data BUS and 4 bits for control. Assume transferring a block from Memory to Processor (or Processor to Memory) takes consecutive 9 cycles (one cycle for information sender, receiver, and address and 8 cycles for data of the cache block). The BUS uses FCFS policy. The 4-bit control is used for (a) processor request line and granted line and (b) Memory request line and granted line. The grant line can be activated for 10 cycles for an request. The abstract view of the processor, memory, and bus connection is shown in Figure B. Assume data send request from memory side are served alternatively from both the channel in round robbin fashion (from channel 0 and channel 1).

Assume consecutive requests are independent and can be served in parallel but each ith access is dependent on all the requests before the i-10th requests.

- Simulate your design using input values and find out the resource usage of your design. *Write a test bench for the same to validate your design using simulation. Trace files for Memory can be generated from the given C++ Code and may be used in test bench designing.*

Part II: Download the Design and Test on the FPGA Boards

- *Instantiate the TestBench as one Processor module "and store the whole traces in a memory" and read one by one and send them to the DRAM module. Generate the total number of page hits and display on the 7-segment display of the FPGA Board.*

Your design should have three separate modules namely **Processor, Memory and Memory Controller**.

Evaluation Procedure

- All the members of the group need to be present at the time of the Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of the demonstration (as it is difficult to remember the faces of all the 128 students in your batch).
- For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires), performance, comments, and questionnaire and explanation

Figure A

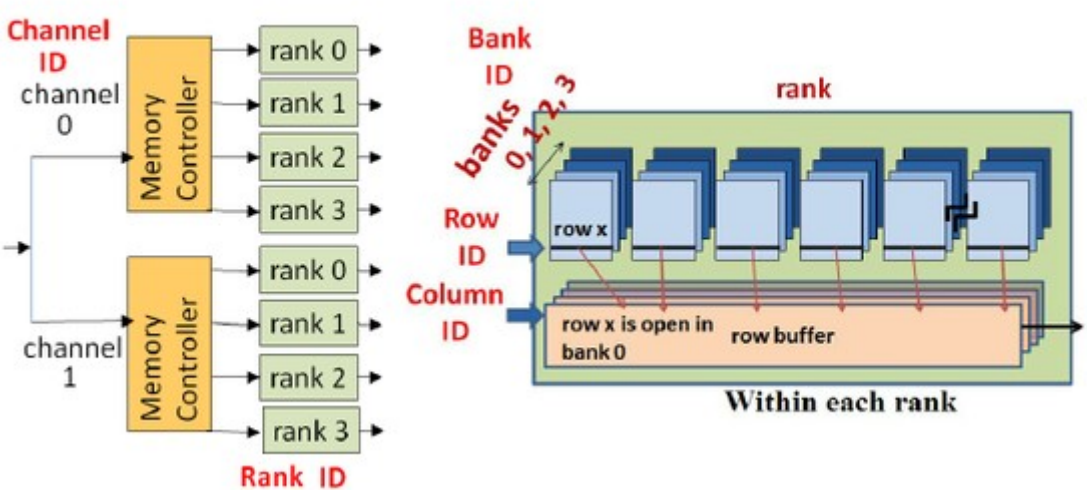

Figure B