# CS224 : Assignment 1
## Date of Demonstration 17th Jan 2023, Lab Timing (2PM-5PM), 10% (5%+ 5%) weight

**Part I (Breadboard and IC part)**

Implement and Demonstrate 4 bit Binary Adder using Breadboard, ICs and Hookup Wires. Y*ou are allowed to use IC7483 4 bit Full Adder.*

**Part II (VHDL and FPGA)**

Implement and Demonstrate 4 bit Binary Adder using HDL (either VHDL or Verilog), synthesize and simulate your design entry. After that Download bit file of your design to FPGA board and demonstrate the working of your design on FPGA.

**Evaluation Procedure**
- All the member of the group need to be present at the time of Demonstration of the assignment. All the absent members will be awarded 0 marks for the assignment. Please show your ID card at the time of demonstration (as it is difficult to remember faces of all the 128 students of your batch).
- Grading will be based on (a) Correctness, (b) Quality of design, (c) Wire optimization, (d) Optimum number of chip used,(e) Cleanliness in design (Wire and Chips should be organized to look good), (f) Use of proper Comment/Naming/Labeling of the wires and (g) Questionnaire and explanation.
- For HDL codes the quality will be based on FPGA minimum resource utilization (Synthesis Report: optimized number of LUTs, register, Minimum Clock), coding style (Use of proper Comment/Naming/Labeling of the wires ), performance, comments, and questionnaire and explanation.

**Helps**

List of IC available in our LAB: http://jatinga.iitg.ernet.in/~asahu/cs223/ICs-HWLAB-CS223.pdf
Installation Procedure for Xilinx ISE/Vivado:
http://jatinga.iitg.ernet.in/~asahu/cs223/ISELicence.txt

Many links are given to VHDL resource at http://jatinga.iitg.ernet.in/~asahu/cs223/

You can take help from TAs. All the TAs and Instructor of CS223 will be available in Lab timing. You can ask TAs or Raktajit Pathak (Room CSE H101) or Bhriguraj Borah (Room CSE Server Room) about licensing and installation of Xillinx ISE/Vivado software.

Breadboard and required ICs may be issued from Hemanta Nath (Hardware Lab). You are not allowed to take Breadboard out of the Hardware Lab. Also required FPGA Board can be issued from Hemanta Nath (Hardware Lab).

We will issue up to two FPGA Boards (Maximum of one BASYS/one ZYBO/one ATLYS/one Nexys A7) for each group for the whole semester. You need to keep the board with you for the whole semester and you are allowed to take issued FPGA board to your Hostel. Based on your requirement, please issue the board from Lab in charge. We have tested working of Xilinx ISE/Vivado on Window 10 and Ubuntu 20/22.04 PC.

You may download/use Vivado 22 and get online user licence from Xilinx Website.