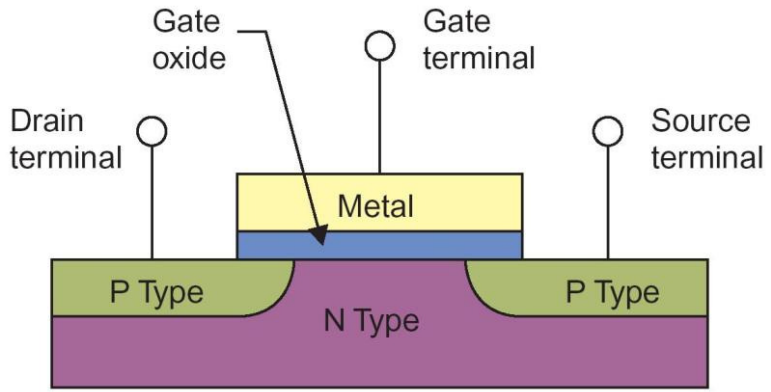
Analog & Digital Electronics

Course No: PH-218

Lec-26: Metal Oxide Field Effect Transistors (MOSFETs)



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Structure of MOSFET

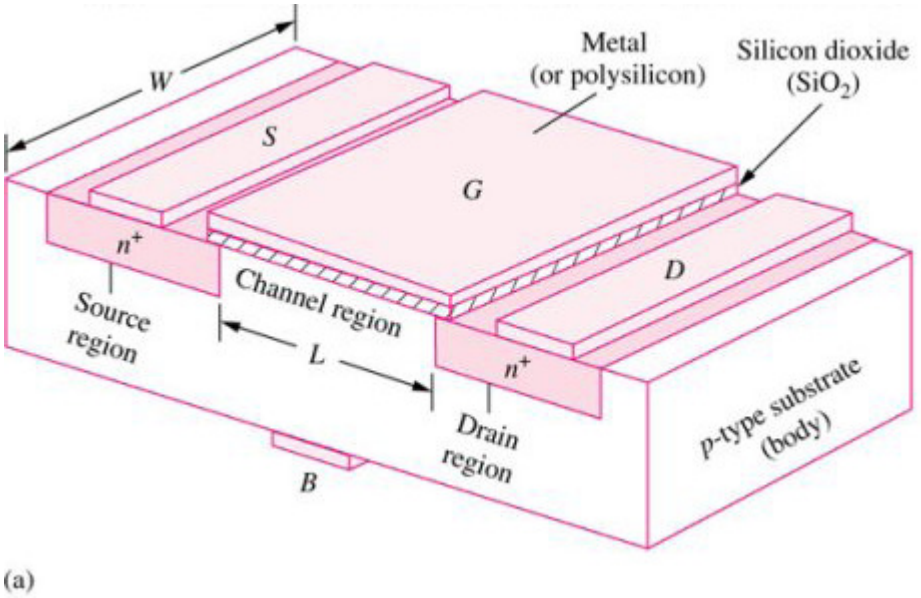
Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is the primary component in high-density chips such as memories and microprocessors

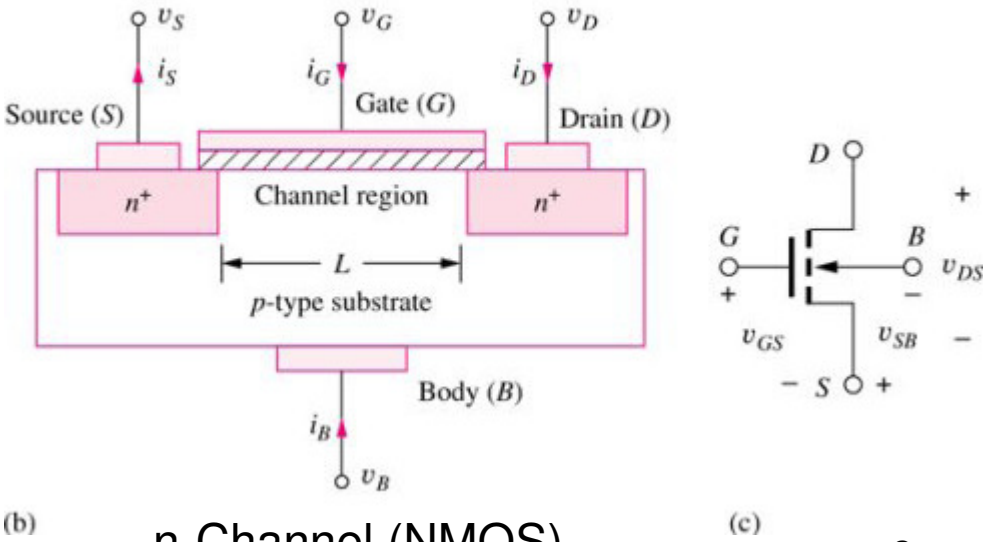
MOSFET is a four terminals FET: **Gate, Source, Drain and body**

Types of MOSFET:

✓ n-Channel (NMOS)
✓ p-Channel (PMOS)

➢ The minimum value of L is referred as the **feature size of** the fabrication technology.

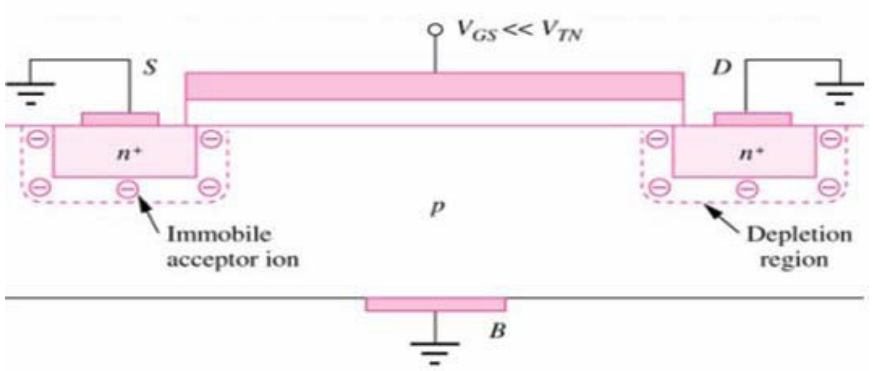


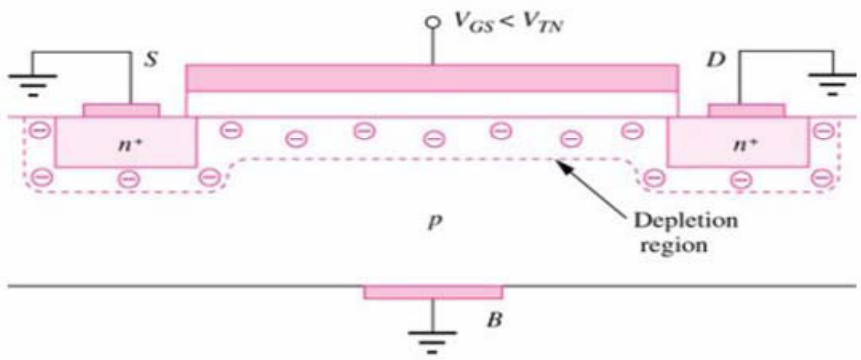


n-Channel (NMOS)

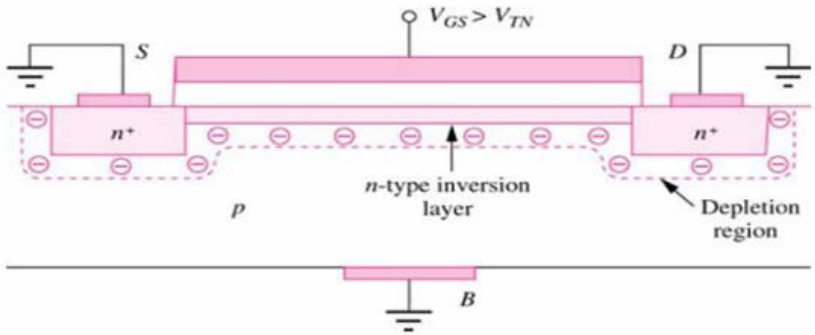
Operation of n channel MOSFET

Body and source are tied to ground. When V_{DS}= 0 and V_{GS}=0, source-body and drain-body diode are off hence no current can flow & MOSFET is in cutoff.





When V_{DS}= 0 and 0 < V_{GS} < V_t ,Vertical electric field established. Holes repelled and depletion region under gate oxide forms.



When V_{DS}= 0 and V_{GS} > V_t, A n type inversion layer formed underneath the gate oxide when V_{GS} reaches a critical value V_t, called threshold voltage. The channel connects source to drain and current flow between them.

Operation of n channel MOSFET

➢ When $V_{GS} > V_t$ and a small V_{DS} is applied

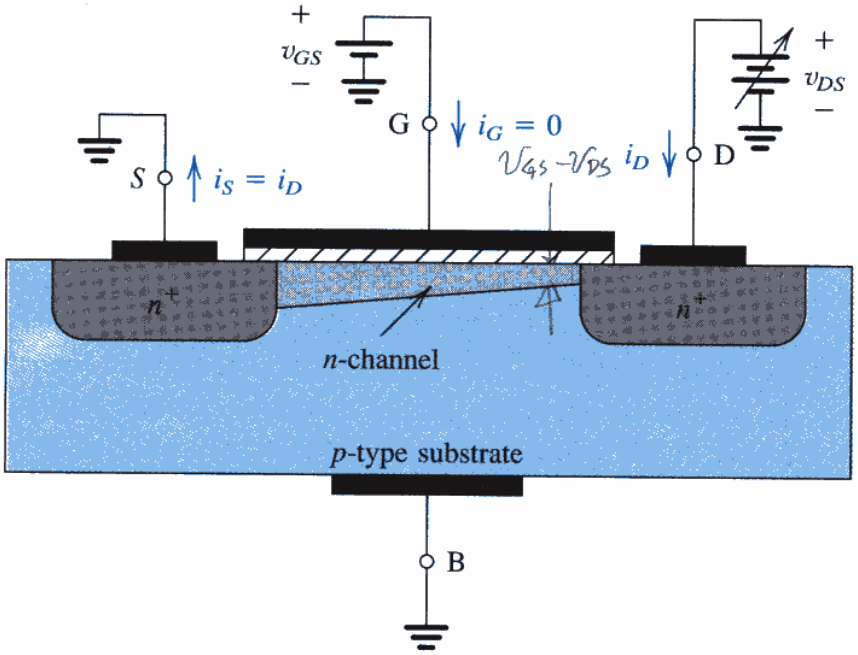
– Current flows from D to S (Electrons flow from S to D) and $I_{DS} \propto V_{DS}$

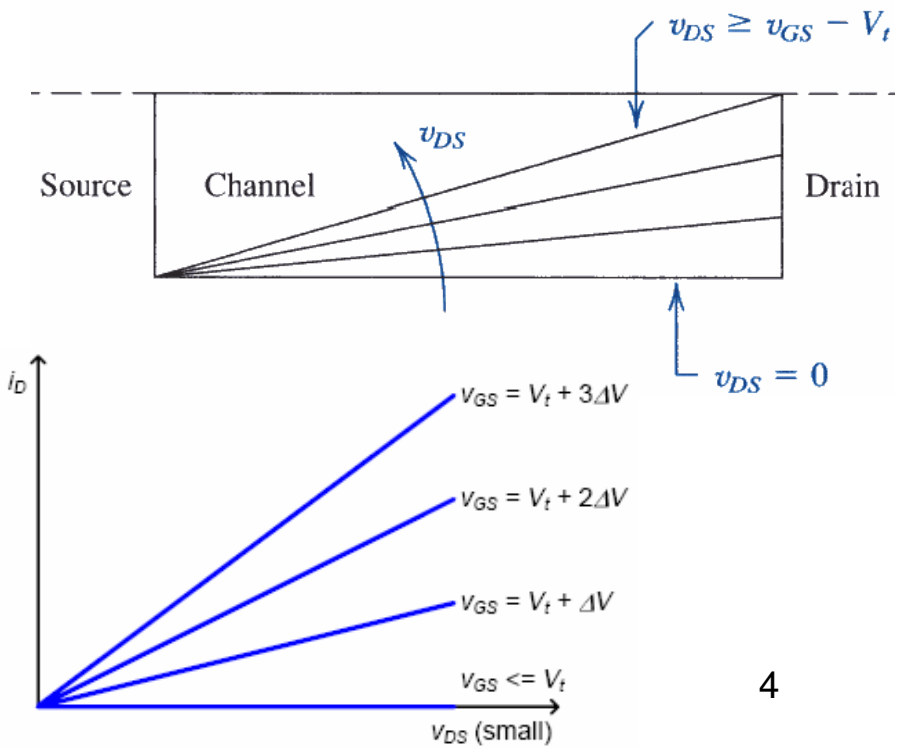
Electric field in the oxide is highest at the source end of channel. Thus many electrons are injected near the source.

Electric field in the oxide is lowest at the drain end of channel. Thus few electrons are induced near the drain.

➢ Increasing V_{GS} above V_t increases the electron density in the channel, and in turn increases the conductivity between D & S, hence I_{DS} increases.

➢ MOSFET behave like a voltage controlled resistor.





Operation of n channel MOSFET

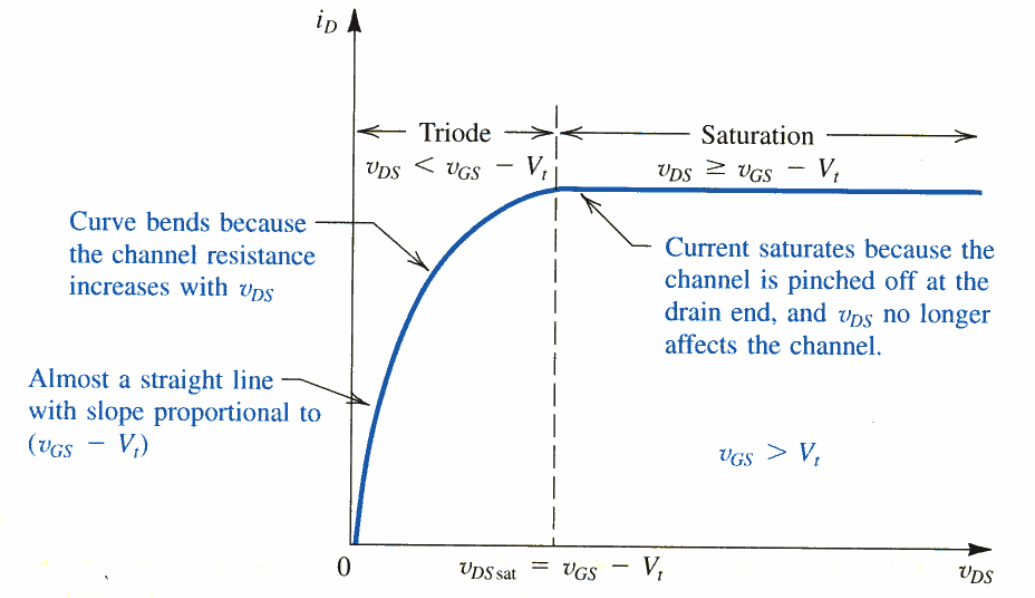
➢ Increase V_{DS} → Decrease V_{GD} → less electrons at the drain side of the channel

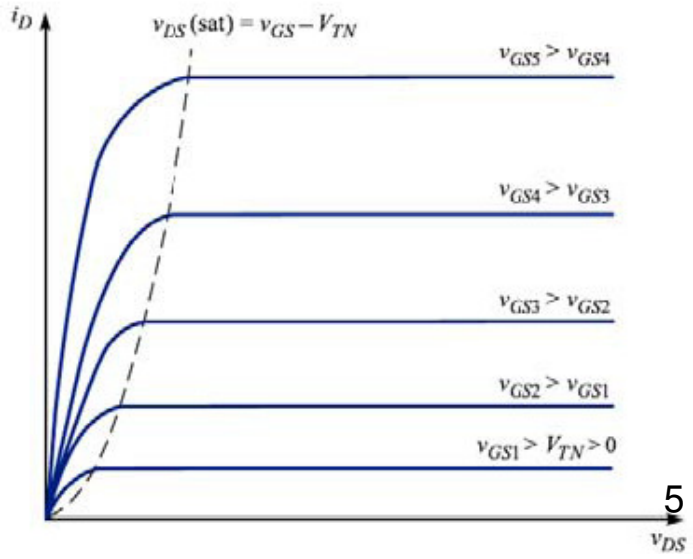
➢ When $V_{DS} \geq V_{GS} - V_t$ then $V_{GD} \leq V_t$ so no channel exists at the drain side. The channel "***pinches-off***"

➢ When channel pinches off, electrons still flows from S to D

✓ Electrons are diffused from the channel to the depletion region near D, where they are drifted by the lateral *E-field to the D*

➢ Further increase of V_{DS} - no effect on the channel - current is "saturated" and the transistor is in "***Saturation Mode***"





I-V Characteristics of n channel MOSFET

➢ MOS structure looks like a parallel plate capacitor and V_{GC} is composed of two components: V_t to form the channel and (V_{GC}-V_t) to accumulate negative charges in the channel.

$$Q_{channel} = CV$$

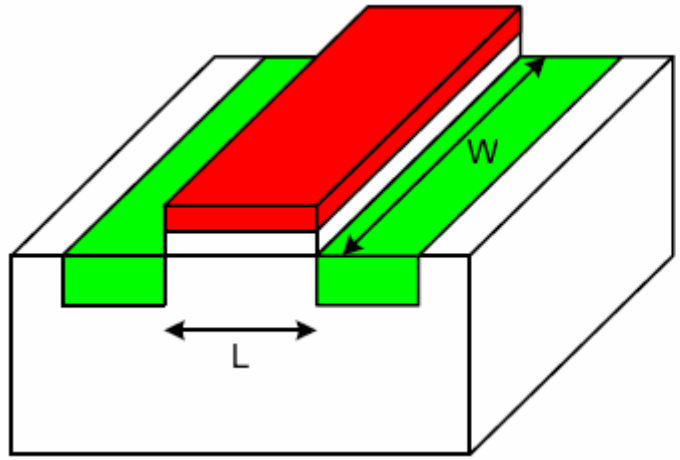
$$C = \frac{\varepsilon_{ox} LW}{t_{ox}} = C_{ox} LW$$

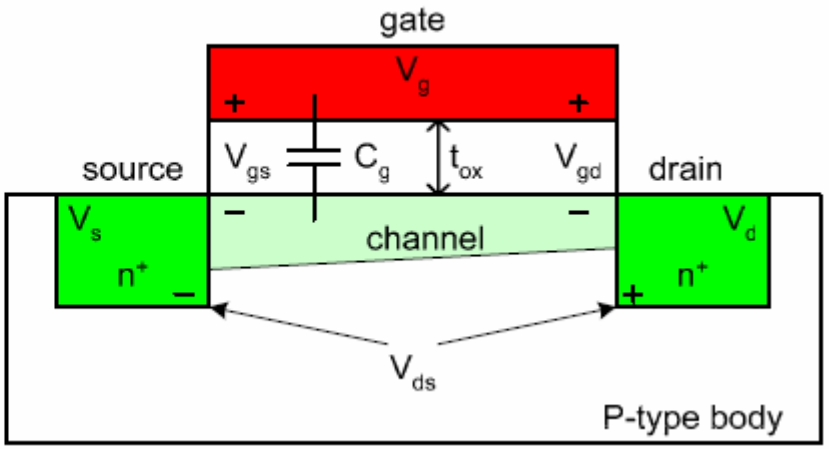
$$V = V_{GC} - V_t = (\frac{V_{GS} - V_{DS}}{2} - V_t)$$

$$v = \mu_n E = \mu_n \frac{V_{DS}}{L}$$

$$t = \frac{L}{v} = \frac{L^2}{\mu_n V_{DS}}$$

Charge is carried by electrons and Carrier velocity v is proportional to the lateral E-field between S and D.





I-V Characteristics of n channel MOSFET

In the Linear region, drain current depends on
– How much charge is in the channel
– How fast the charge is moving

$$I = \frac{Q_{channel}}{t}$$

$$I = \frac{\mu_n C_{ox} W}{L}[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2]$$

For $V_{GS} > V_t$ and $V_{DS} \geq V_{dsat} = V_{GS} - V_t$: I_D is independent of V_{DS}

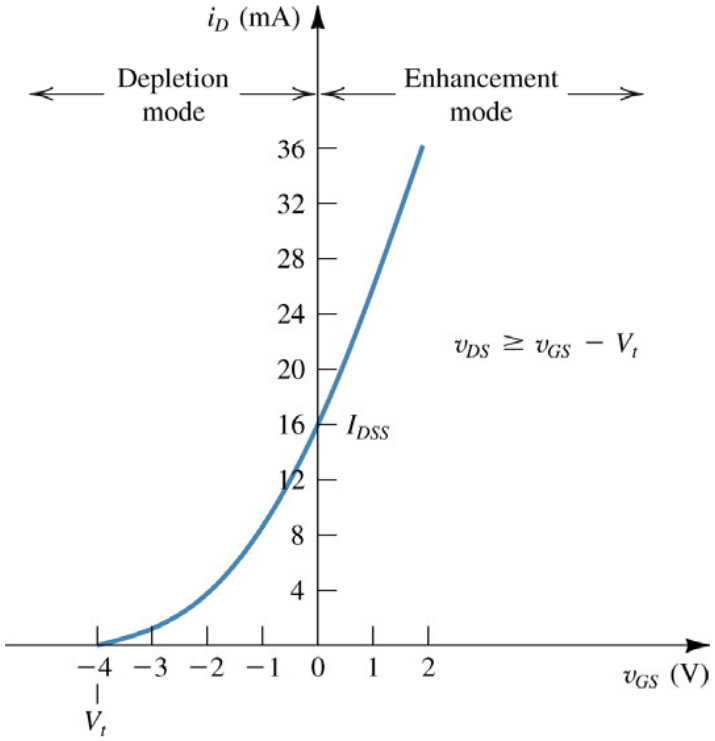
In Saturation mode

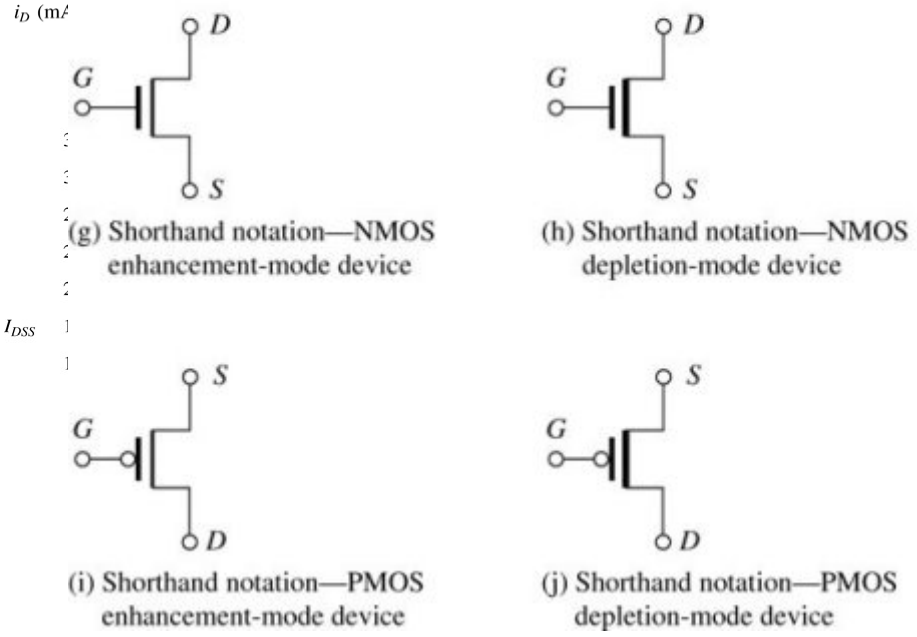
$$i_D = \frac{1}{2}(\mu_n C_{ox})\frac{W}{L}(v_{GS} - V_t)^2$$

Depletion and Enhancement mode MOSFET

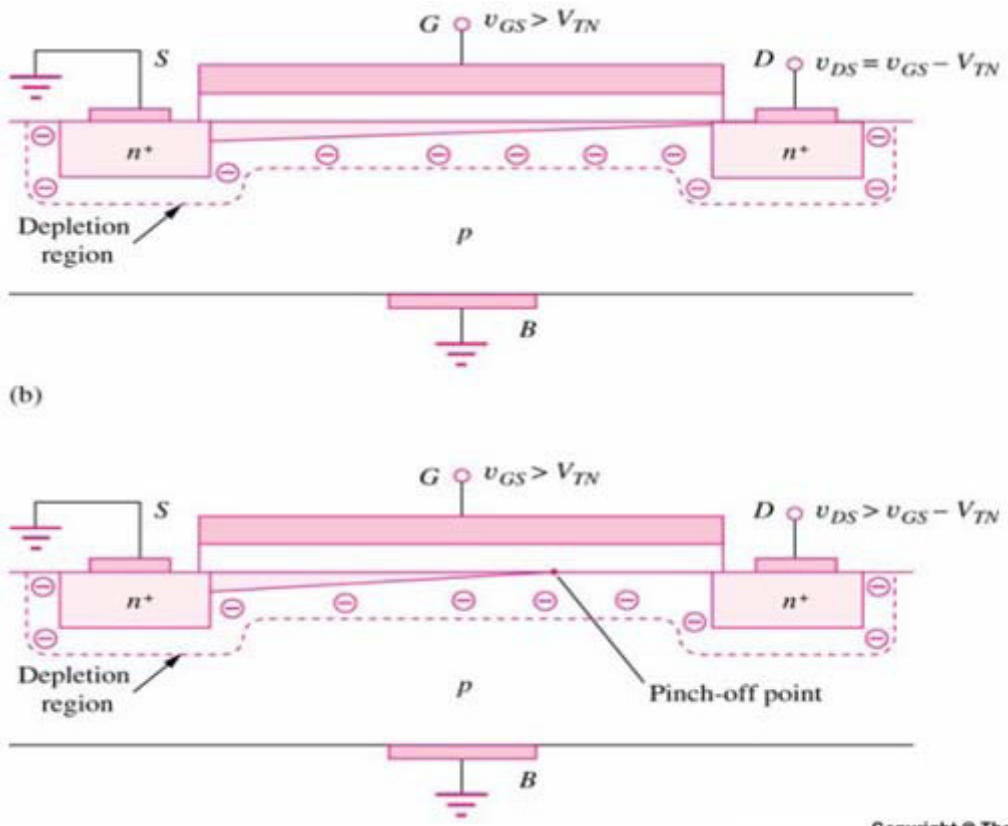
- A depletion-type MOSFET has a built-in channel by fabrication i.e. It is ON when no gate-source voltage is applied and need to apply a negative V_{GS} to turn off device. V_t is negative for NMOS.

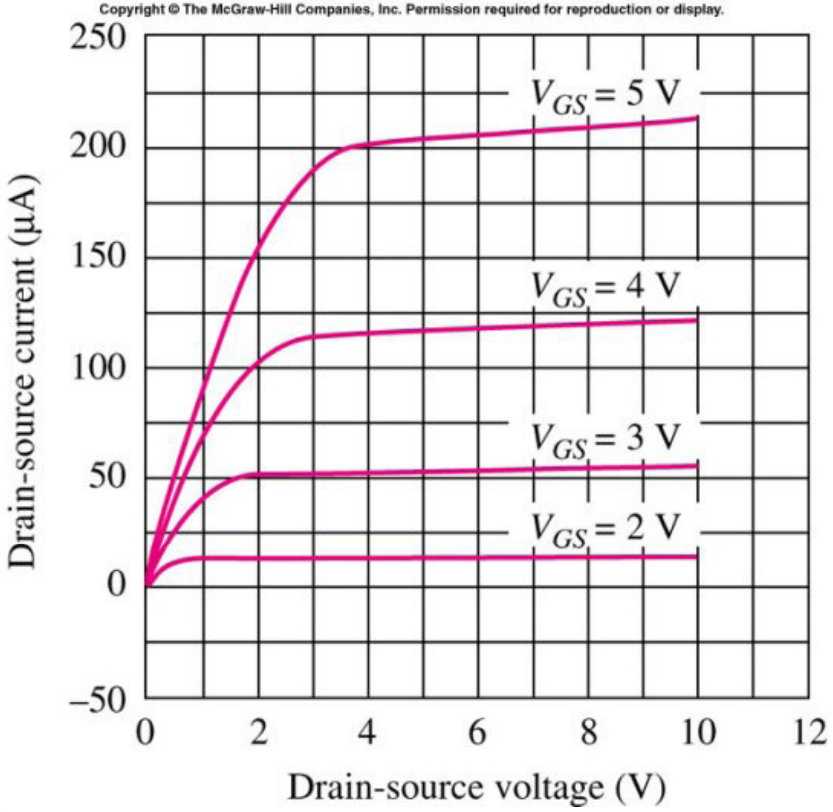
- MOSFET is said to be enhancement type if gate-source voltage is applied to turn on the transistor. V_t is positive for NMOS.



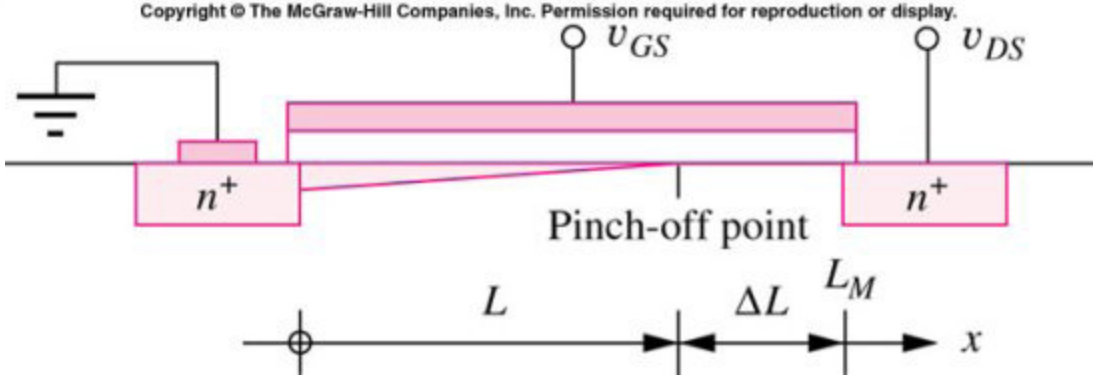


Channel length Modulation

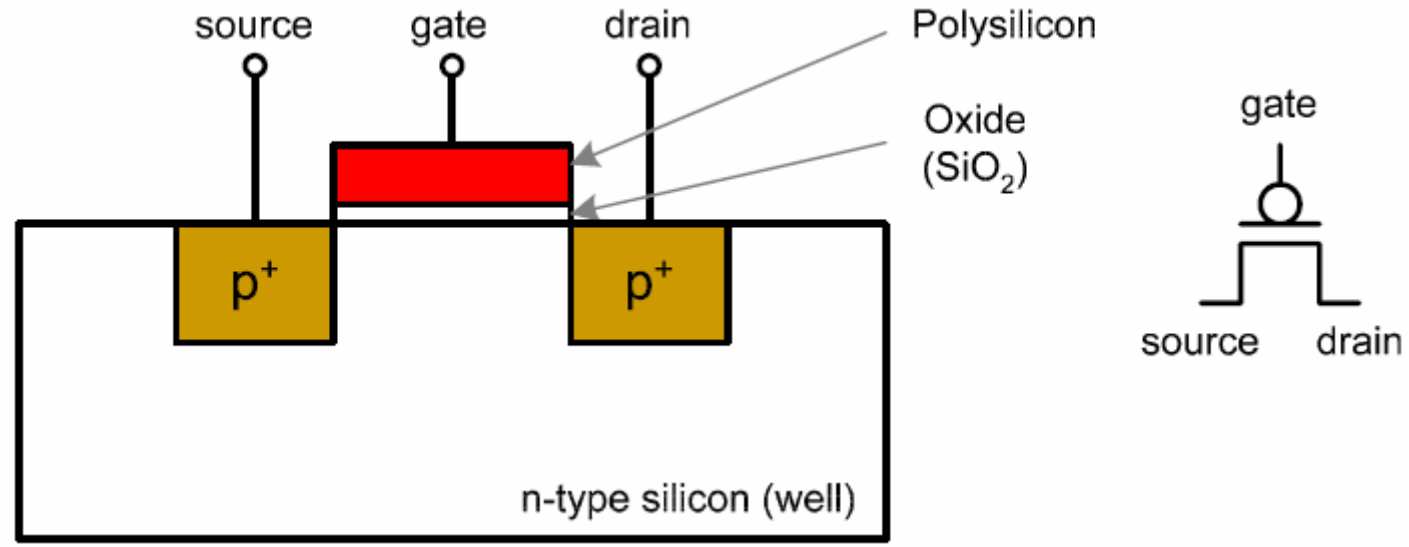


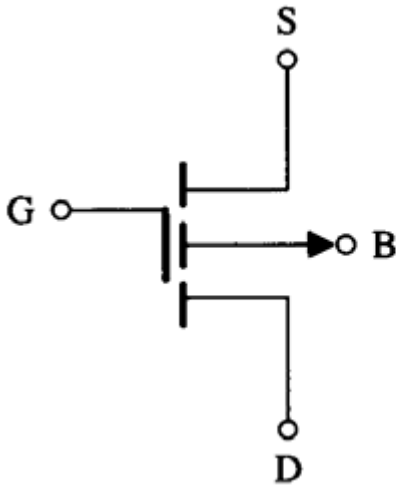


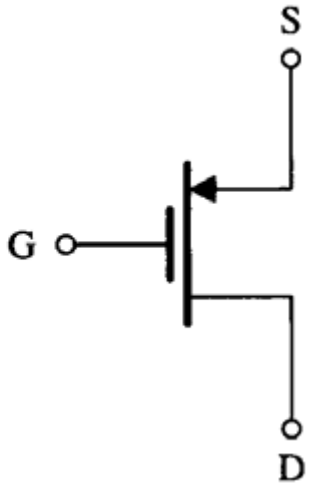
The effective channel length L is reduced by ΔL and hence I_{DS} increases.



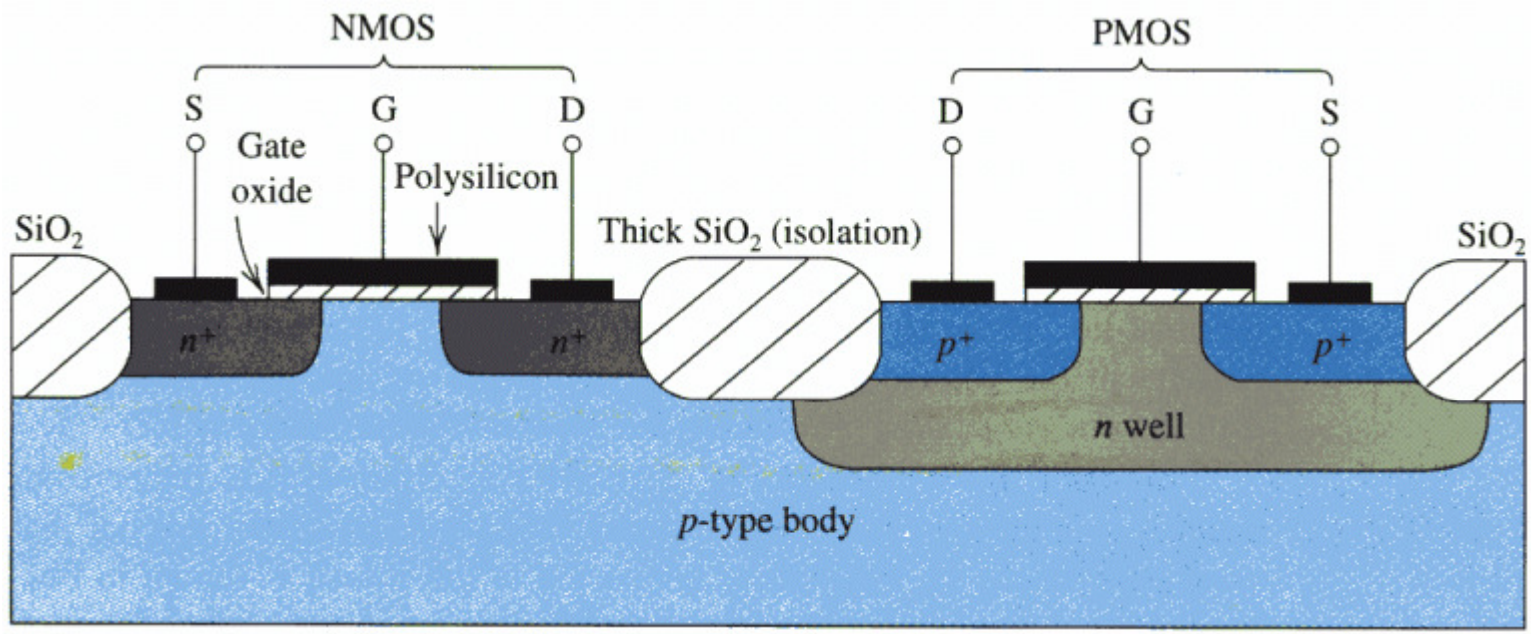
P-channel MOSFET (PMOS)







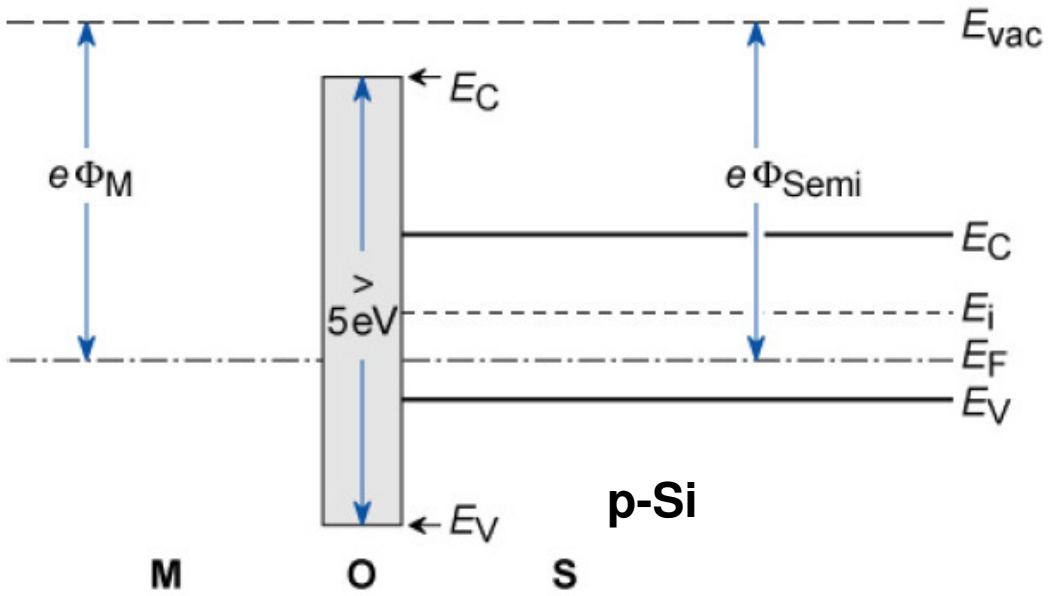
Complimentary MOSFET (CMOS)



Complementary MOS or CMOS integrated-circuit technologies provide both NMOS and PMOS on a same IC

Supplement slide: How inversion layer forms?

(1) $V_G = 0$ (Equilibrium)
(E_F = constant throughout structure)



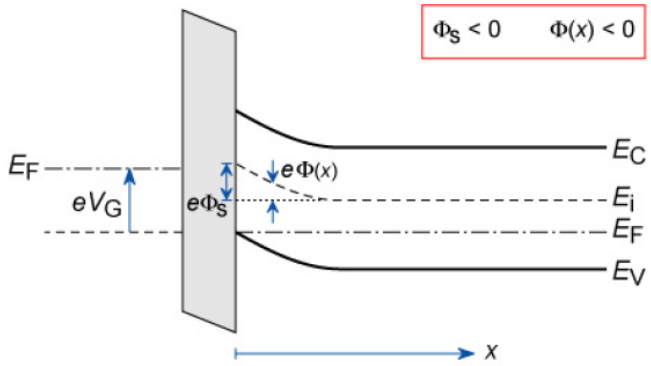
Reference: E.F. Schubert, Renesselaer Polytechic Institute 2003

Supplement slide: Accumulation ($V_G < 0$)

(2) When $V_G < 0$ (Accumulation):

Gate bias is –ve so E_f at the gate goes up. Since M and S have much higher conductivity than O so voltage between Gate and channel mostly drops at oxide. An Electric field will be generated at oxide.

Band diagram:



Fermi levels are different in M and S.

Fermi levels are constant within M and within S.

Recall that

$$p(x) = n_i e^{(E_i - E_F)/kT} \quad (1)$$

$p(x)$ increases near the surface → Accumulation (*i. e.* we have an accumulation of holes near the surface)

Definition of surface potential = Φ_S

Surface potential energy = $e\,\Phi_S$ = difference of bulk value of E_i and surface value of E_i

Reference: E.F. Schubert, Renesselaer Polytechic Institute 2003

Supplement slide: Accumulation ($V_G < 0$)

When bands bend upwards:

$$E_i^{bulk} - E_i^{surface} = e\Phi_S < 0$$

When bands bend downwards:

$$E_i^{bulk} - E_i^{surface} = e\Phi_S > 0$$

Under flatband conditions:

$$\Phi_S = 0$$

Introducing dependence of the potential Φ on the position x:

$$e\,\Phi(x) = E_i^{bulk} - E_i(x)$$

$$\Phi_S = \Phi(x = 0)$$

$$p(x) = n_i \, e^{(E_i - E_F)\,/\,kT}$$

$$= n_i \, e^{[E_i^{bulk} - e\Phi(x) - E_F]\,/\,kT}$$

$$= n_i \, e^{(E_i^{bulk} - E_F)\,/\,kT} \, e^{-e\,\Phi(x)\,/\,kT}$$

$$p(x) = p_0 \, e^{-e\,\Phi(x)\,/\,kT}$$

Since $\Phi(x) < 0$, $p(x)$ increases close to the surface.

That is, we have accumulation.

Reference: E.F. Schubert, Renesselaer Polytechic Institute 2003

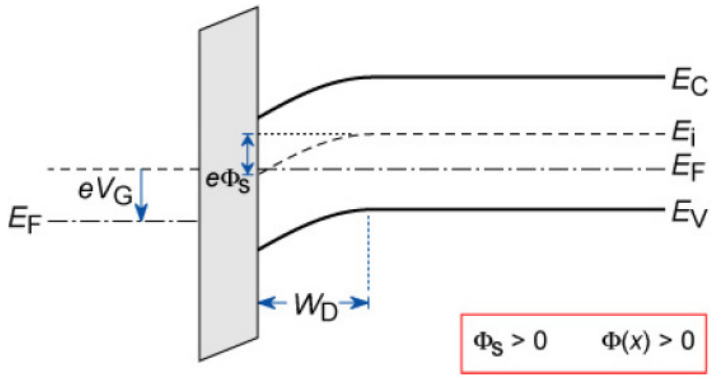
Supplement slide: Depletion ($V_G > 0$)

(3) $V_G > 0$ (Depletion)

The gate bias is positive.

E_F "goes down" in the metal.

Band diagram:



Semiconductor is depleted near surface.

The depletion layer thickness follows from Poisson's equation:

$$W_D = \sqrt{\frac{2\varepsilon}{eN_A}\Phi_S} \qquad (8)$$

E_F is near E_i at the surface.

➔ Semiconductor is practically intrinsic at the surface.

Recall Eq. (7): $p(x) = p_0\, e^{-e\Phi(x)/kT}$

It is $\Phi(x) > 0$ ➔ $p < p_0$, that is, we have a depleted layer near the surface.

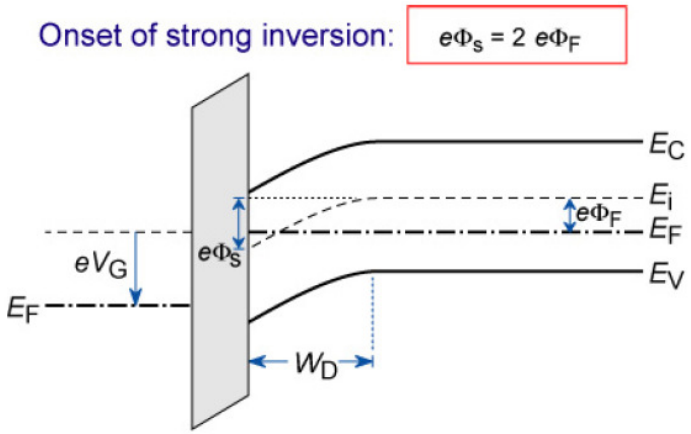
Reference: E.F. Schubert, Renesselaer Polytechic Institute 2003

Supplement slide: Inversion ($V_G >> 0$)

(4) $V_G >> 0$. (Onset of strong inversion)

The gate bias is position.

E_F goes further down in metal.



Semiconductor is depleted of holes near surface.

E_F is closer to E_C than to E_V at the surface.

➔ Semiconductor is n-type near surface

➔ Conductivity type of semiconductor is inverted.

Criterion for the onset of strong inversion:

$$e\Phi_S = 2e\Phi_F \quad \text{(Onset of strong inversion)}$$

where

$$e\Phi_F = E_i^{bulk} - E_F^{bulk}$$

Onset of strong inversion means that the semiconductor is as strongly n-type at the surface as it is p-type in the bulk.

Using Boltzmann statistics

$$p = n_i \, e^{(E_i - E_F)/kT} \qquad (11)$$

and Eqs. (9) and (10), one obtains

$$e\Phi_S = 2e\Phi_F = 2kT \ln\frac{N_A}{n_i} \quad \text{(Onset of strong inversion)} \quad (12)$$

At the onset of strong inversion, an n-channel begins to be formed at the semiconductor surface.

Reference: E.F. Schubert, Renesselaer Polytechic Institute 2003