Information Security Education and Awareness Project Phase II

BILATERAL / INTERNATIONAL COOPERATION

Workshop on Advances in Hardware Security

24th - 29th May, 2019.

Organised by

Dept. of Computer Science and Engineering, IIT Guwahati.

ELIGIBILITY, REGISTRATION AND SELECTION

The workshop is open to

- **Faculty from academic and technical institutions.**
- **Persons from R&D organisations/industries and staff working in R&D projects.**
- **Student from CSE/ECE/IT background (B.Tech./M.Sc./MCA/M.Tech./Ph.D.).**

Registration fee is INR 1000 for participants from ISEA undertaking organisations, and INR 2360 (INR 2000 + 18% GST) for participants from Non-ISEA undertaking organisations. The registration fee will be refunded to the participants from ISEA undertaking organisations, subject to complete participation in the workshop. The registration fee paid will not be refunded to the participants who fail to attend the workshop. There will be a total of 40 seats for the workshop which will be filled based on first come first serve basis.

Please refer the link https://www.isea-pmu.in/home/ for the list of ISEA undertaking organisations.

BOARDING AND LODGING

For participants from ISEA undertaking organisations, accommodation can be arranged free of cost either in the IITG guest house or student hostels inside IITG campus, based on requests from the applicants. Accommodation is from 23.05.19 to 30.05.19. Registration fee will cover course materials and working lunch during the workshop days. Participants can have breakfast and dinner from hostels or guest house on payment basis.
Participants from Non-ISEA undertaking organisations should make their own arrangements for boarding and lodging, although stay at IITG hostels and guest house can be arranged on a payment basis subject to availability of rooms.

TA/DA will not be paid to the participants.

HOW TO APPLY

Interested candidates can find application form, registration details and guidelines in the workshop's website link:
http://www.iitg.ac.in/johnjose/isea_ahs.html

Duly filled application form, and the registration fee Demand Draft drawn in favour of "Registrar, IIT Guwahati", payable at Guwahati should be sent to the program convener Dr. John Jose by speed post. Last date for receipt of application form and registration fee DD is 25.04.2019. List of selected candidates after Round-I will be displayed on the website by 30.04.2019.

IITG ISEA COORDINATOR

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ABOUT IIT GUWAHATI

Indian Institute of Technology Guwahati (IITG) [http://www.iitg.ac.in], the sixth member of the IIT fraternity was established in 1994. IITG has been able to build up world class infrastructure for carrying out advanced research and has been equipped with state-of-the-art scientific and engineering instruments. IITG campus is on a sprawling 285 hectares plot of land on the north bank of the river Brahmaputra around 20 kms from the heart of the city. The Department of Computer Science and Engineering [http://www.iitg.ac.in/cse], started its academic program in the year 1995 and is celebrating 25th year of its inception. It provides an outstanding research environment complemented by excellence in teaching. The department offers B.Tech., M.Tech., Ph.D. and Dual (M.Tech. + Ph.D.) degree programs. The department has around 30 faculty members actively involved in various cutting edge research domains in Computer Science field.

ABOUT ISEA

Keeping in view the pervasive nature and impact of cyber security on all walks of life - economic and social, Government of India has identified Information Security as one of the major thrust area for launching various development programs. One of the key elements essential for information security is availability of right kind of qualified and well trained human resources, who could take up Research & Development (R&D), develop indigenous solutions / software, secure and maintain various systems including critical infrastructure. The purpose of ISEA projects is to achieve this through various Education, Awareness and Training programs.

ABOUT THE WORKSHOP

The perspective of the workshop is to generate quality human resource to enhance the research and development in the field of hardware security through a short course consisting of several lectures and interactive discussion sessions. The course will touch upon several fundamental questions in this field and stimulate interest in students and researchers to explore further. The objectives of the workshop are:

- To teach principles of security and trust verification from System-on-Chip (SoC) perspective.
- To equip students with industry standard skills relating to designing SoCs using third party IPs, and how to verify their security using a combination of formal methods, testing techniques and side-channel analysis.
- To provide a clear picture of how formal verification techniques (such as model checking, equivalence checking and theorem proving) can be effectively employed for both pre-silicon and post-silicon validation of SoC security and trust.
- To explore the synergy between logic testing and side channel analysis for detecting hardware Trojans in IoT devices from both pre-silicon and post-silicon perspectives.
- To understand key challenges of security of IoT devices, interplays between security and other IoT design parameters, such as observability (debug friendliness), power and reliability.
- To explore and understand security solutions for diverse IoT devices including how industry is approaching in this space. Students will learn the major research topics and the areas, which need major innovations.
- To understand challenges, and solutions in the hardware security field. It will describe practical experiments and labs to train future engineers and users of IoT devices about the security issues and measures to protect themselves and the nation.

WORKSHOP CONTENTS

Day 1: Overview of SoC Design Methodology
Day 2: Hardware Security Vulnerabilities and Countermeasures
Day 3: Formal Verification of Security and Trust
Day 4: Security Validation using Side-Channel Analysis
Day 5: SoC Supply Chain Security

RESOURCE PERSON

Prabhat Mishra is a Professor in the Department of Computer and Information Science and Engineering at the University of Florida, where he leads the CISE. His research interests include embedded and cyber-physical systems, hardware security and trust, energy-aware computing, formal verification, system-on-chip validation, and post-silicon debug. He received his Ph.D. in Computer Science and Engineering from the University of California, Irvine in 2004. Prior to joining University of Florida, he spent several years in various companies including Intel, Motorola, Synopsys and Texas Instruments. He has published 7 books, 25 book chapters, and more than 150 research articles in premier international journals and conferences. Prof. Mishra currently serves as an Associate Editor of ACM Transactions on Design Automation of Electronic Systems (TODAES), IEEE Transactions on Very Large Scale Integration Systems (TVLSI), and Journal of Electronic Testing (JETTA). He is also serving as an ACM Distinguished Speaker. Prof. Mishra is an ACM Distinguished Scientist and a Senior Member of IEEE.