PROGRAM SCHEDULE
(Date wise programme)

DAY-1 (22 November 2013)

09:00AM : Registration

10:00AM : Inauguration and address by Director (IITG), Guest of honour, Deputy Director and Head (EEE).

11:00AM : *Tea*

11:30AM : Presentation on FPGA architecture & Design flow: Xilinx perspective. Concepts of On Chip Debugging using Xilinx Chipscope -Pro (ILA & VIO).

01:00PM : *Lunch*

02:00PM : On Plan Ahead based flow and Concepts of Hardware debugging using ILA and VIO.

03:30PM : *Tea*

04:00PM : Xilinx ISE design flow and Hardware Implementation.

05:00PM : Day-1 Concluding Session

DAY-2 (23 November 2013)

09:00AM : Xilinx Embedded Design flow.

10:30AM : *Tea*

11:00AM : Demonstration of Xilinx Embedded Design flow using XPS and SDK.

12:00AM : Concepts of Hardware modeling – use of Matlab and Simulink and Integrating with Xilinx DSP Design flow using System Generator for DSP.

01:00PM : *Lunch*

02:00PM : Concepts of System modeling and HDL Generation using System Generator; Xilinx DSP Design flow and concepts of Hardware co-simulation; Demonstration of Hardwar co-simulation.

03:45PM : *Tea*

04:00PM : Introduction to Zynq Architecture and Embedded Design flow using Zed board (demonstration); Xilinx Vivado Design flow and features of Vivado HLS – Demonstration of Vivado tool flow and overview of Vivado HLS.

05:00PM : Concluding Session