EE514: VLSI Lab III

- 1. Introduction to Verilog Design and Small Design Implementations to understand Verilog and EDA tools required for the lab.
- 2. Design of 8-Bit Adder, 32-Bit Adder and Multiplier
- 3. Single-Cycle MIPS Datapath
- 4. Single-Cycle MIPS Control
- 5. Single-Cycle MIPS Branches
- 6. 5-Stage MIPS Processor (Pipelining)
- 7. Adding a Simple Branch Predictor to MIPS Processor
- 8. Implementing Full Forwarding to MIPS Processor

Lab Project