Analog & Digital Electronics

Course No: PH-218

BJT

Lec-6: I-V characteristics and Ebers-Moll Model

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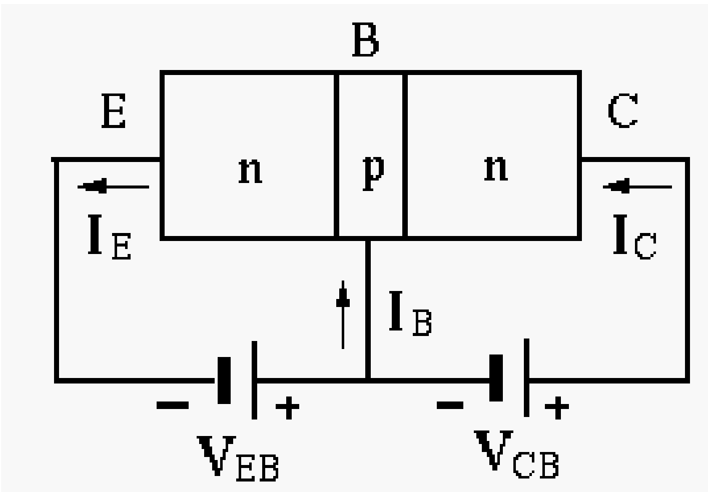
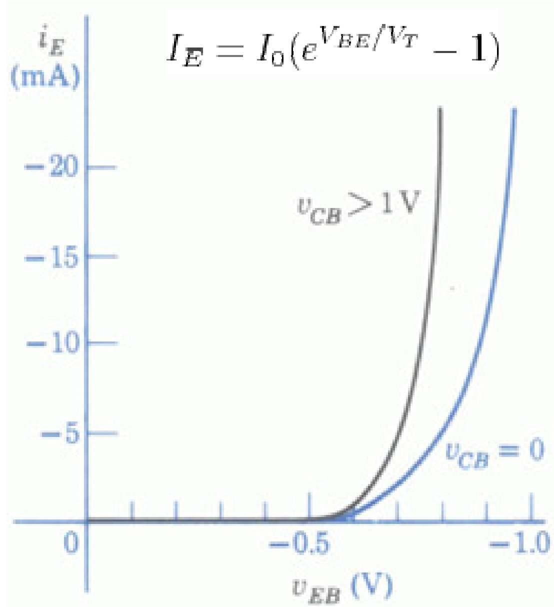
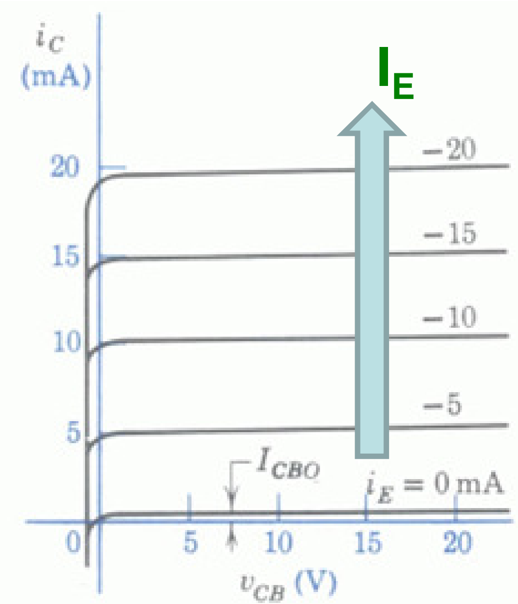
I-V Characteristics of BJT under common base configuration

Common Base configuration





Input characteristics



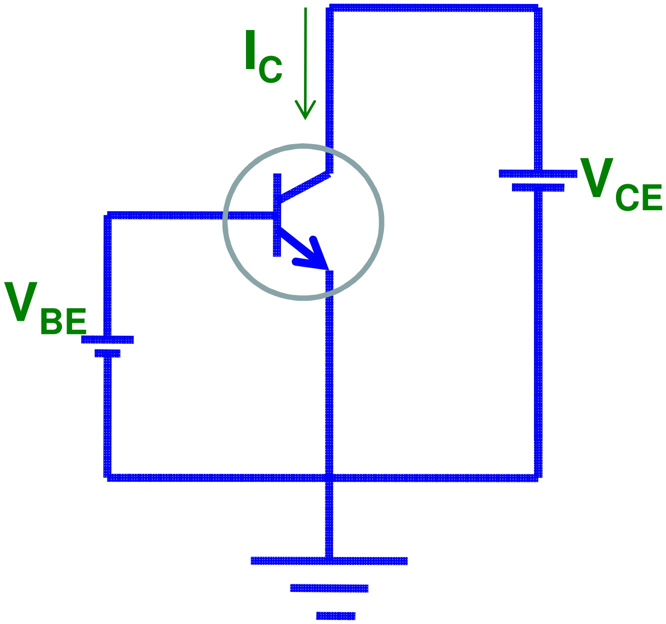
Output characteristics

- Input characteristics are like a normal forward biased diode.
- As the CB junction is reverse biased, the current I_C is independent of collector voltage and depends only upon the emitter current I_E. The collector current is almost constant and work as a current source.
- When I_E=0 , I_C=I_{CB0} is the leakage current caused by the minority carriers crossing the pn-junction.

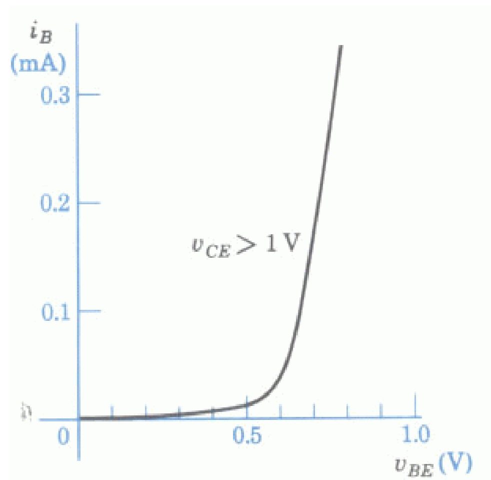
$$I_C = \alpha I_E + I_{CB0}$$

I-V Characteristics of BJT common emitter configuration

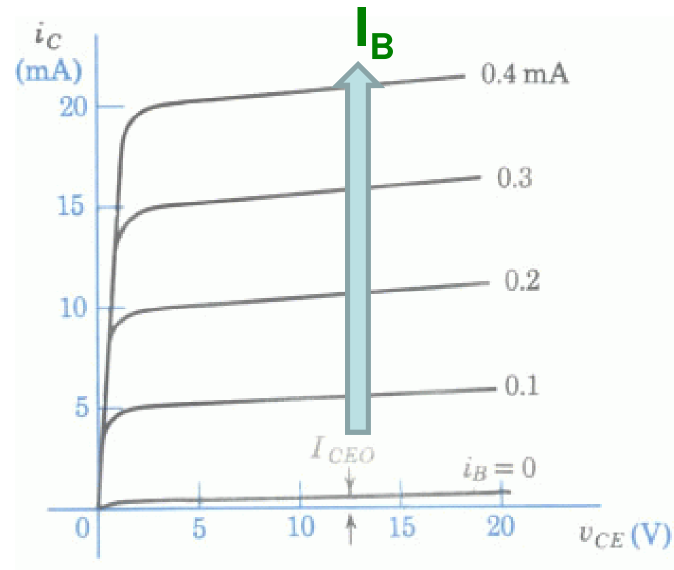
npn common emitter



Input characteristics



Output characteristics



➢ Input characteristics are like a normal forward biased diode.

➢As the CE junction is reverse biased, the current I_C is independent of collector voltage and depends only upon the base current I_B.

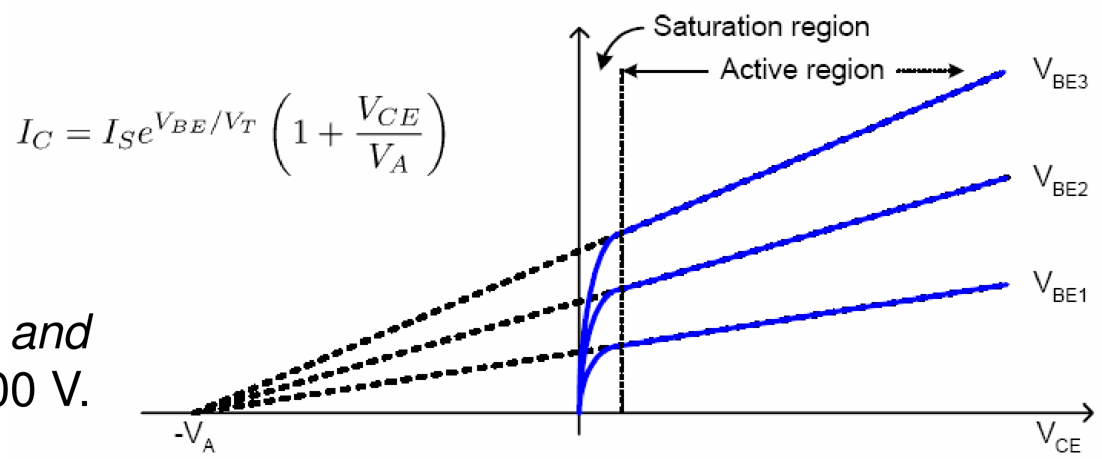
➢ In real diode, the collector current slightly increases with increase in collector emitter voltage(Early effect).

➢ At low value of V_{CE}, the CBJ becomes forward-biased and the transistor enters the saturation region.

Early Effect (Base width modulation)

Observed by James Early

$$I_C = I_s\, e^{\left(\frac{eV_{BE}}{kT}\right)}\left[1+\frac{V_{CE}}{V_A}\right]$$

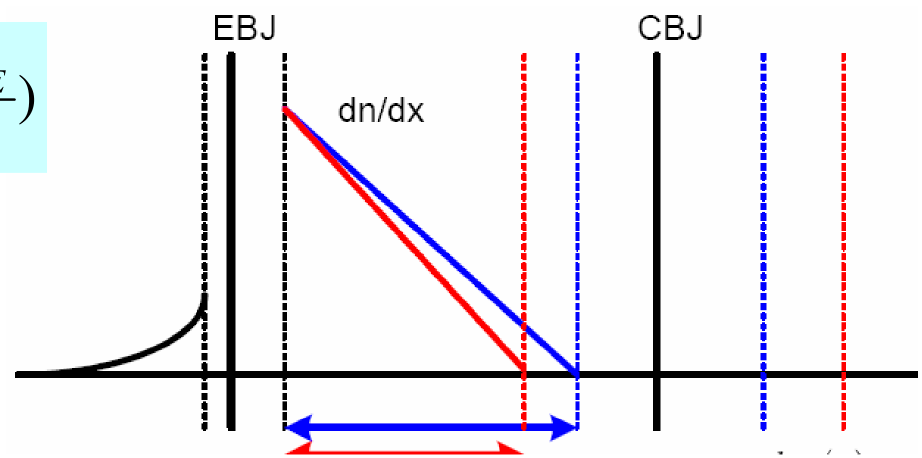


V_A is called the Early voltage and ranges from about 50 V to 100 V.

Early effect can be modeled as

$$I_C = I_c' + \frac{V_{CE}}{r_o}$$ *where* $$I_c' = \mathrm{I_s}\exp\left(\frac{eV_{BE}}{kT}\right)$$

$$r_o \equiv \left[\frac{\partial i_C}{\partial v_{CE}}\bigg|_{v_{BE}=\text{constant}}\right]^{-1} \qquad r_o = \frac{V_A}{I_C'}$$

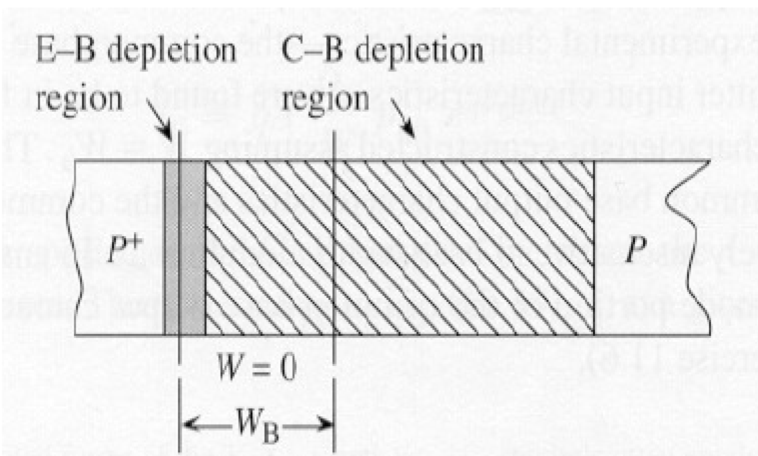


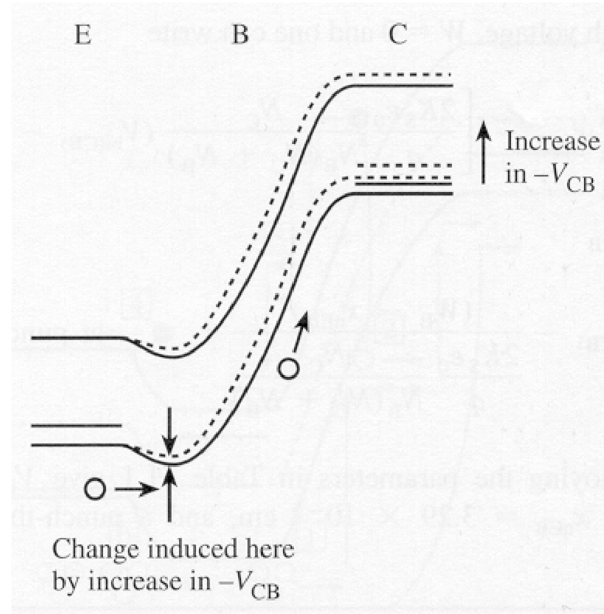
- When V_{CB} increases:
- ❖ depletion region of CBJ widens
- ❖ so the effective base width decreases (base-width modulation)

V_{CB} > V_{CB}

Base punch through

➢ if reverse bias voltage of C-B junction is keep on increasing, a situation arises where E-B and C-B space charge regions touch each other, and the width of the quasi-neutral base region becomes zero, Known as base punch through.

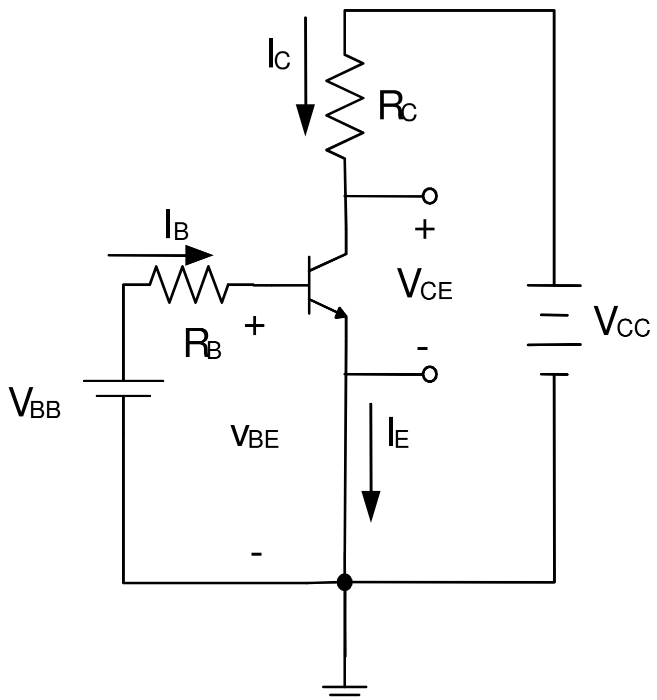


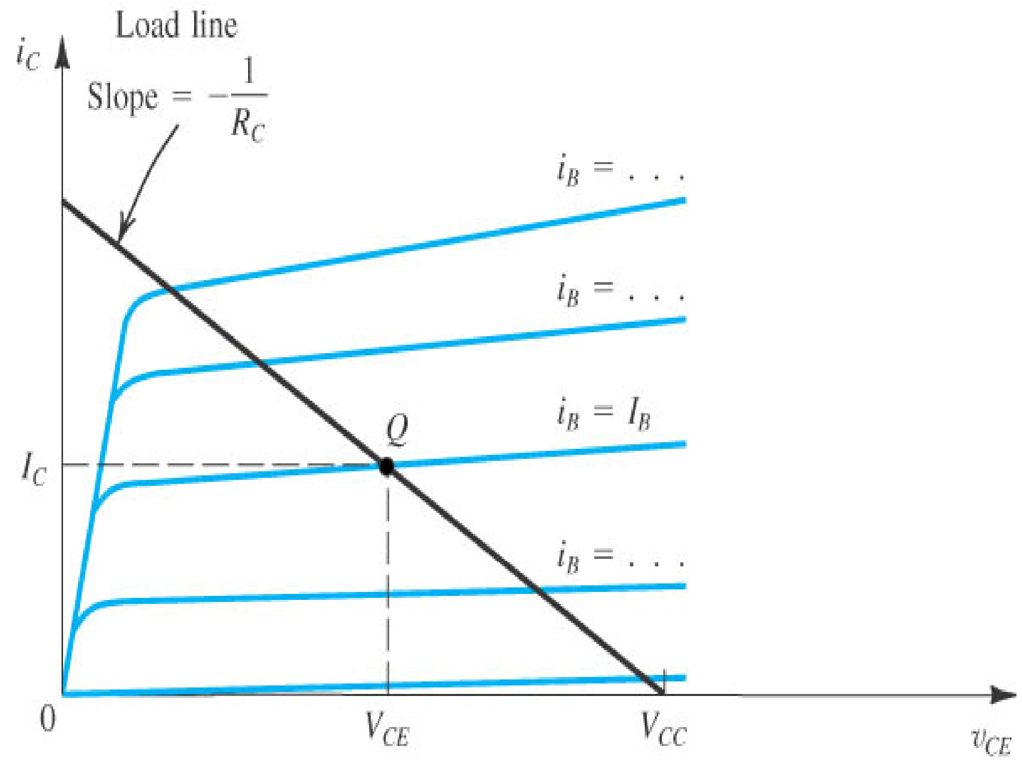


➢ Any increase in V_{CB} beyond the punch-through point lowers the E-B potential barrier and allows a large injection of carriers from the emitter directly into the collector.

➢If punch-through occurs, the maximum voltage (V_{CB0} or V_{CE0}) that can be applied to a BJT is limited.

DC Load Line Analysis





Application of KVL in output (CE)circuit:
$V_{CE} = V_{CC} - I_C R_C$; is called Load line equation.
When $I_C = 0$, $V_{CE} = V_{CC}$; When $V_{CE} = 0$, $I_C = V_{CC}/R_C$

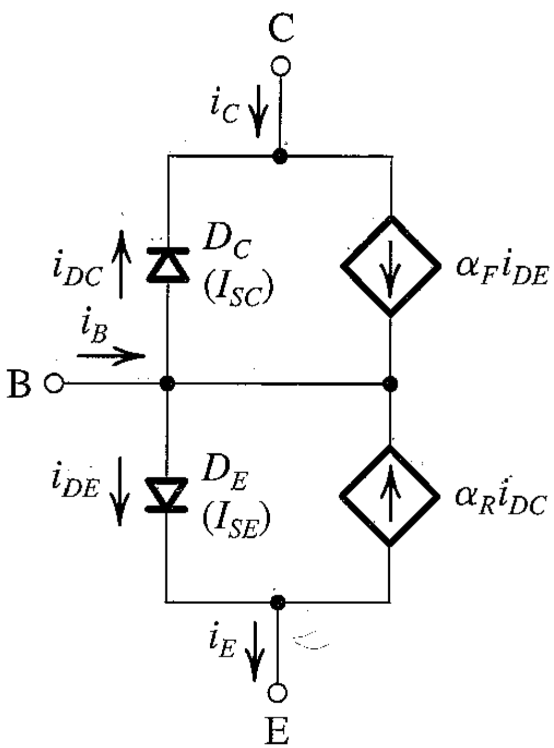
- **The operating point Q (V_{CEQ}, I_{CEQ}) is determined by finding the intersection point of load line and BJT output characteristics for a particular value of base current.**

Ebers-Moll Model (Large-Signal Model)

➢ The Ebers-Moll (EM) model is a large-signal model for BJT. It relates the transistor d.c terminal currents to voltages.

➢ EM model is low frequency (static) model based on the fact that BJT is composed of two pn junctions – EB and CB junction.

➢ Therefore terminal currents of BJT can be expressed as a superposition of the currents due to the two pn junctions.

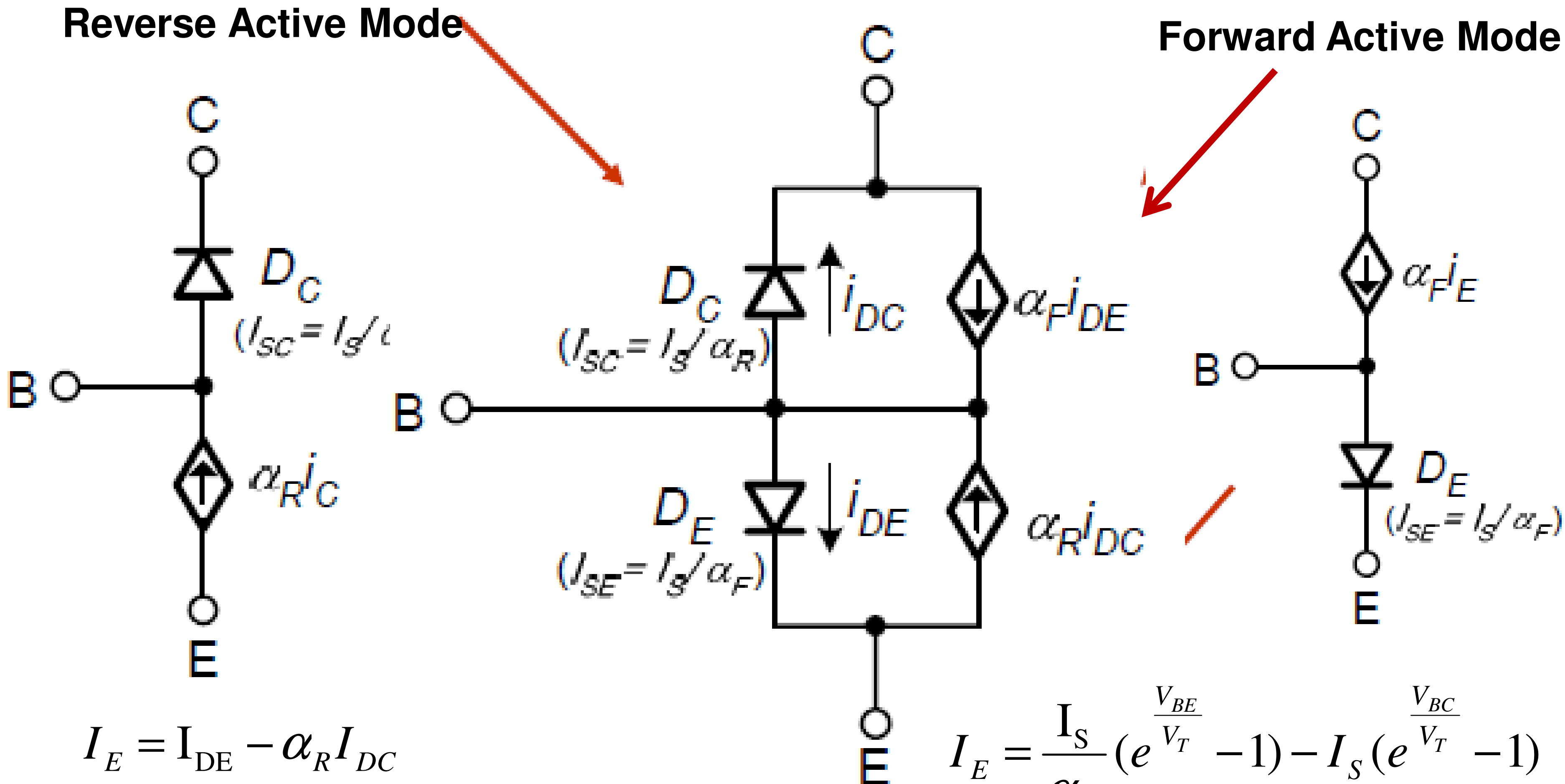


D_E : E-B junction diode
D_C : C-B junction diode

$$I_{DE} = I_{SE}(e^{\frac{V_{BE}}{V_T}} - 1) \qquad I_{DC} = I_{SC}(e^{\frac{V_{BC}}{V_T}} - 1)$$

$$I_{DE} = \frac{I_C}{\alpha} = \frac{I_S}{\alpha}(e^{\frac{V_{BE}}{V_T}} - 1) = I_{SE}(e^{\frac{V_{BE}}{V_T}} - 1)$$

Ebers-Moll Model (Large-Signal Model)



$$I_E = I_{DE} - \alpha_R I_{DC}$$

$$I_C = -I_{DC} + \alpha_F I_{DC}$$

$$I_B = (1-\alpha_F) I_{DE} + (1-\alpha_R) I_{DC}$$

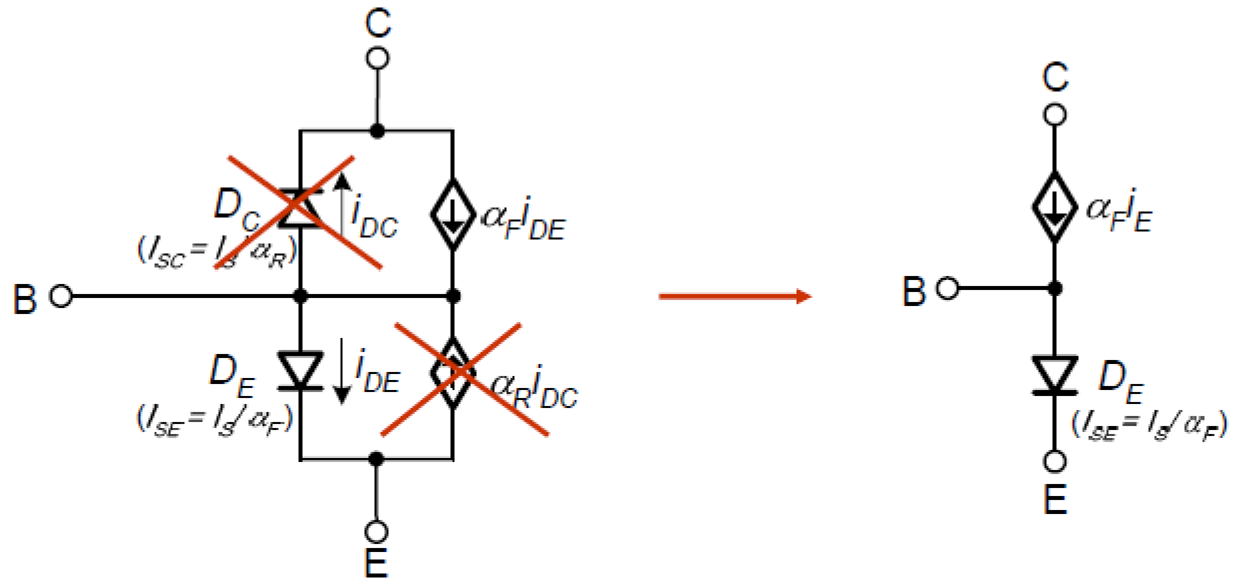
$$I_E = \frac{I_S}{\alpha_F}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - I_S\left(e^{\frac{V_{BC}}{V_T}} - 1\right)$$

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \frac{I_S}{\alpha_R}\left(e^{\frac{V_{BC}}{V_T}} - 1\right)$$

Ebers-Moll Model (Large-Signal Model)

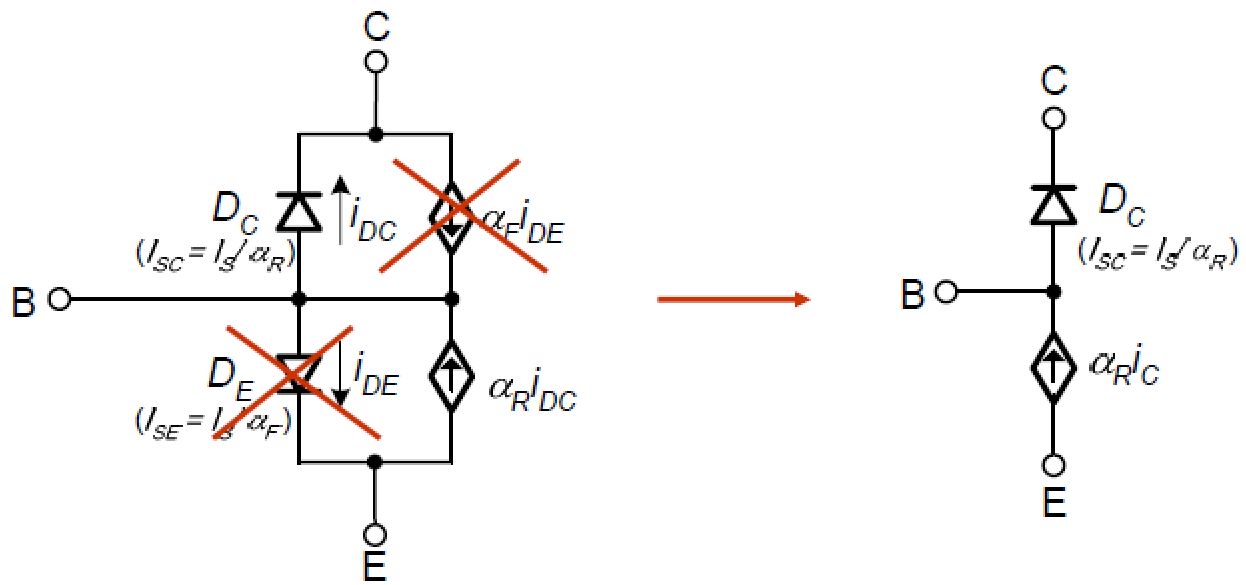
BJT Forward Active Mode

BE forward-biased,
BC reverse-biased:



BJT Reverse Active Mode

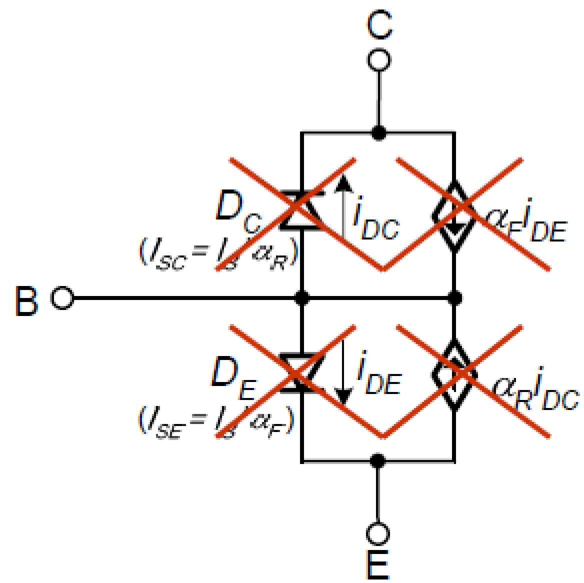
BE reverse-biased,
BC forward-biased:

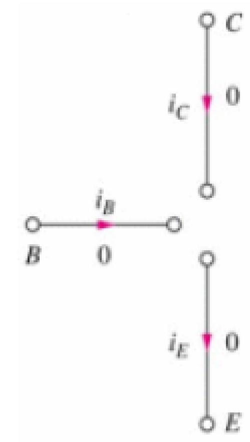


Ebers-Moll Model (Large-Signal Model)

BJT Cut-off Mode

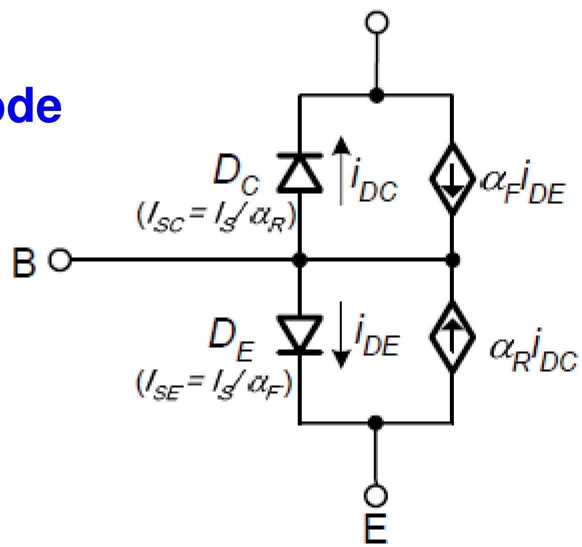
BE reverse-biased,
BC reverse-biased:



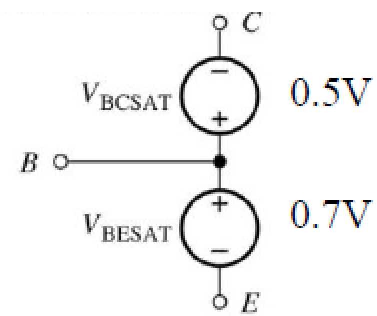


BJT Saturation Mode

BE forward-biased,
BC forward-biased:

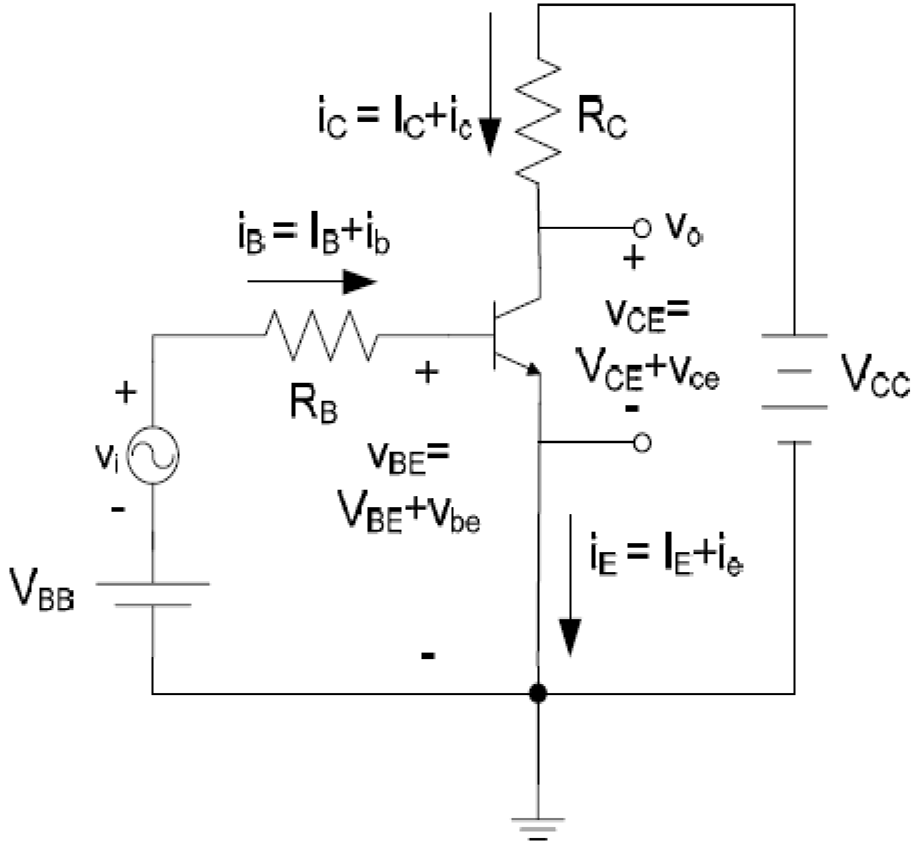


Diodes simplified as constant voltage drops.



Their parallel current sources can be omitted.

BJT with input ac signal



$i_B = I_B + I_b$
$i_E = I_E + i_e$
$i_C = I_C + i_c$

I_B, I_C,I_E - D.C. currents
I_b, i_c, i_e – A.C. currents
i_B, i_C, i_E – D.C + A.C. currents

Similarly,
V_{BE}, V_{CE} – D.C. Voltages
v_{be}, v_{ce} – A.C.Voltages
v_{BE}, v_{CE} – D.C+ A.C Voltages

Biasing schemes for BJT

➢ Biasing refers to the application of D.C. voltages to setup the operating point in such a way that output signal is undistorted throughout the whole operation.

➢ Also once selected properly, the Q point should not shift because of change of I_C due to

(i) β variation
(ii) Temperature variation

Different biasing schemes

(i) Fixed bias (base resistor biasing)
(ii) Collector base bias
(iii) Emitter bias
(iv) Voltage divider bias

$$I_E = \mathrm{I}_{\mathrm{DE}} - \alpha_R I_{DC}$$

$$I_C = -\mathrm{I}_{\mathrm{DC}} + \alpha_F I_{DC}$$

$$I_B = (1 - \alpha_F)\mathrm{I}_{\mathrm{DE}} + (1 - \alpha_R) I_{DC}$$

$$I_E = \frac{\mathrm{I}_{\mathrm{S}}}{\alpha_F}\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - I_S\left(e^{\frac{V_{BC}}{V_T}} - 1\right)$$

$$I_C = I_S\left(e^{\frac{V_{BE}}{V_T}} - 1\right) - \frac{\mathrm{I}_{\mathrm{S}}}{\alpha_R}\left(e^{\frac{V_{BC}}{V_T}} - 1\right)$$