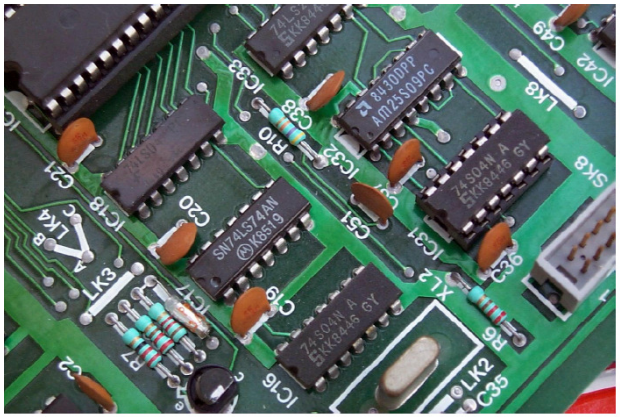
Analog & Digital Electronics

Course No: PH-218

Lec-29: CMOS Logic Family



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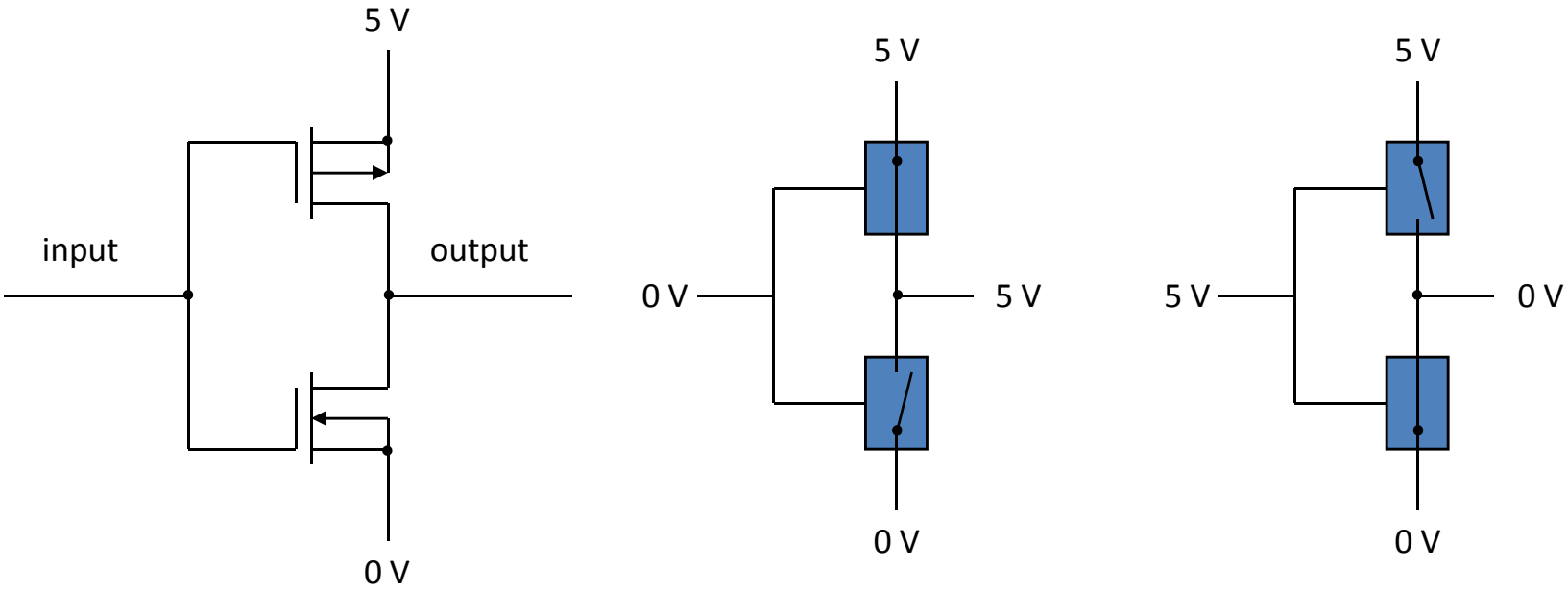
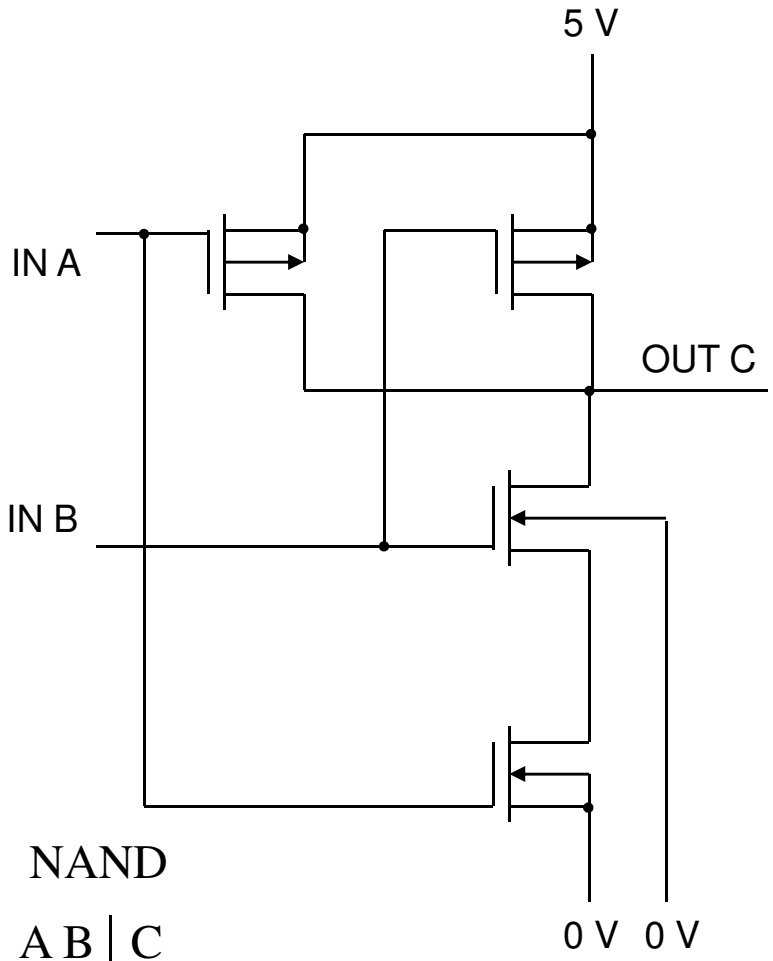
MOSFETs as an inverter



- 0 V input turns OFF lower (n-channel) FET, turns ON upper (p-channel), so output is connected to +5 V
- 5 V input turns ON lower (n-channel) FET, turns OFF upper (p-channel), so output is connected to 0 V
  - Net effect is logic inversion: 0 → 5; 5 → 0
- Complementary MOSFET pairs → CMOS

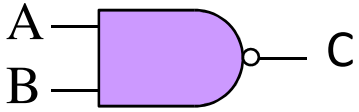
NAND gate from MOSFETs

Lower two FETs are NMOS and Upper two FETS are PMOS.



NAND

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0



When Both Inputs A & B at zero:

- ✓ Lower two NMOS is OFF, Upper two PMOS is ON – resulting output C at HI

When Both Inputs A & B at 5V (HI):

- ✓ Lower two NMOS is ON, Upper two PMOS is Off – result in output C at LOW.

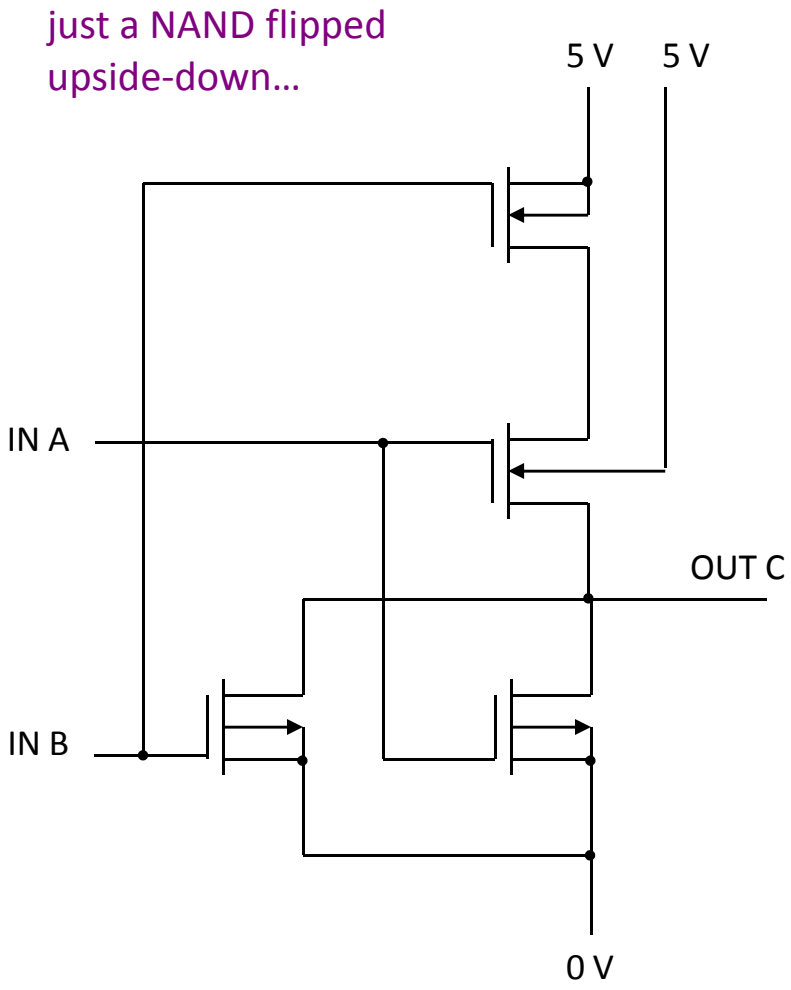
When Inputs A at 5V & B at 0V:

- ✓ upper left OFF, lowest ON
- ✓ upper right ON, middle OFF
- ✓ result is output HI

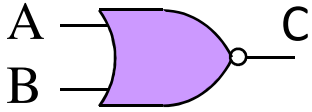
When Inputs A at 0V & B at 5V:

- ✓ upper left ON, lowest OFF
- ✓ upper right OFF, middle ON
- ✓ result is output HI

NOR gate from MOSFETs



- Both inputs at zero:
  - lower two FETs OFF, upper two ON
  - result is output HI
- Both inputs at 5 V:
  - lower two FETs ON, upper two OFF
  - result is output LOW
- IN A at 5V, IN B at 0 V:
  - lower left OFF, lower right ON
  - upper ON, middle OFF
  - result is output LOW
- IN A at 0 V, IN B at 5 V:
  - opposite of previous entry
  - result is output LOW



NOR

A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

Input/Output Voltage of MOS logic family

- **VOHmin :** The minimum output voltage in HIGH state (logic '1') = 4.7V for CMOS
- **VOLmax :** The maximum output voltage in LOW state (logic '0') = 0.2V for CMOS
- **VIHmin :** The minimum input voltage in HIGH state (logic '1') = 3.7 V for CMOS

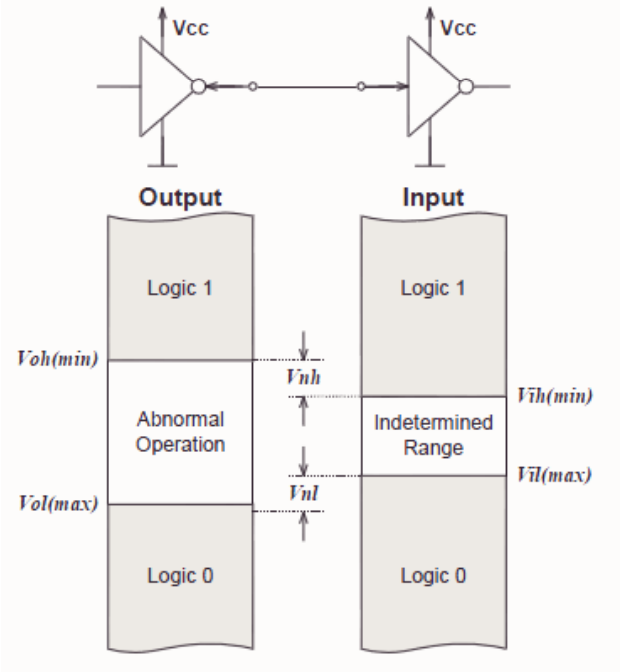
VILmax : The maximum input voltage in LOW state (logic '0') = 1.3 V for CMOS

Low noise margin (LNM):

$LNM = VI_{Lmax} - VO_{Lmax} = 1.3 - 0.2 = 1.1V$

High noise margin(HNM):

$HNM = VO_{Hmin} - VI_{Hmin} = 4.7 - 3.7 = 1.0V$



Input/Output Current of MOS logic family / Fan-out

When a CMOS driver output is LOW, the maximum input current to the CMOS load is only 1uA. This means CMOS driver has to sink only 1uA. ($I_{IL,\ max}$ = -1uA)

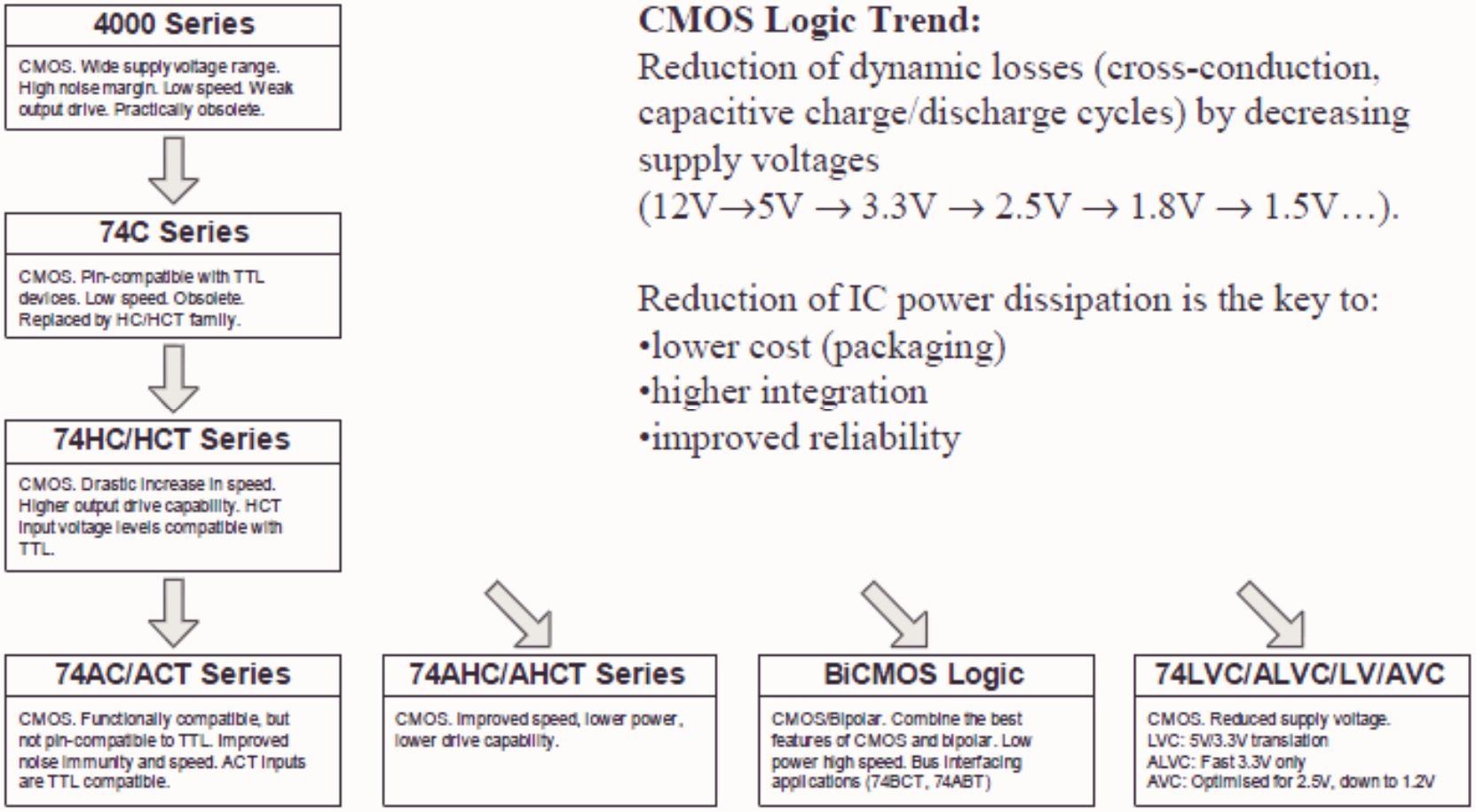
Similarly when CMOS driver output is high, the CMOS driver is sourcing 1uA. ($I_{IH,\ max}$ = 1uA)

To determine fan-out, one must know how much input current gate load draws (I_{in}) and how much output current the driving gate can supply (I_o).

For 74C00 series, output current for CMOS driving CMOS:
$I_{OL,\ max}$ = 10uA and $I_{OH,\ max}$ = - 10uA

Fan-out under HIGH & LOW condition is same and equal to 10.

Evolution of CMOS Logic Family



CMOS Logic Trend:

Reduction of dynamic losses (cross-conduction, capacitive charge/discharge cycles) by decreasing supply voltages
(12V→5V → 3.3V → 2.5V → 1.8V → 1.5V…).

Reduction of IC power dissipation is the key to:

- lower cost (packaging)
- higher integration
- improved reliability

Comparison between CMOS & TTL Logic Family

TTL: transistor-transistor logic: BJT based

chips have L, LS, F, AS, ALS, or H designation

output: logic high has $V_{OH} > 3.3$ V; logic low has $V_{OL} < 0.35$ V

input: logic high has $V_{IH} > 2.0$ V; logic low has $V_{IL} < 0.8$ V

dead zone between 0.8V and 2.0 V

nominal threshold: $V_T = 1.5$ V

CMOS: complimentary MOSFET

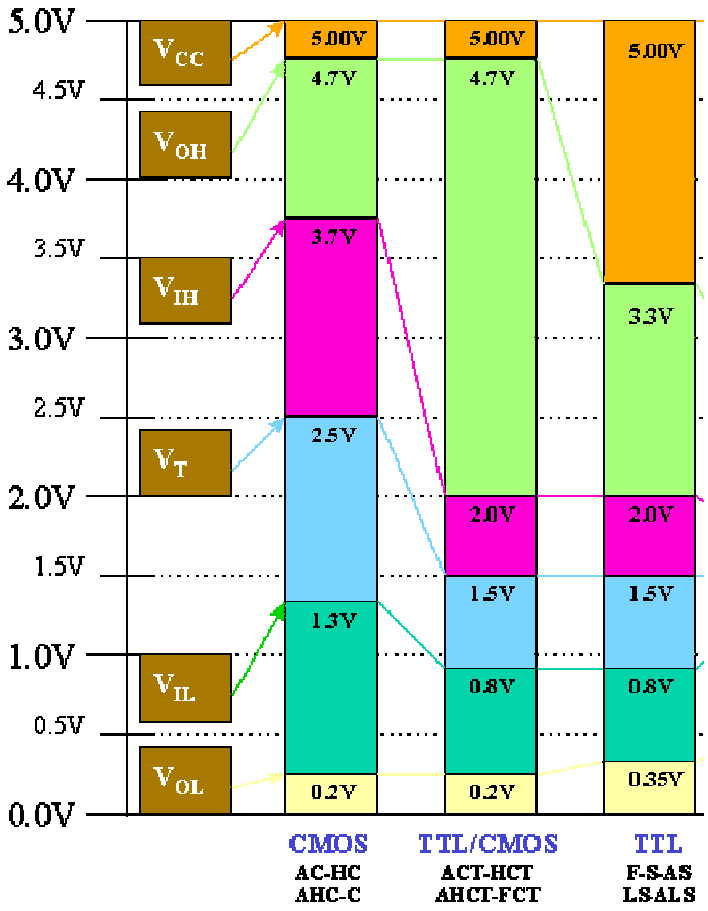
chips have HC or AC designation

output: logic high has $V_{OH} > 4.7$ V; logic low has $V_{OL} < 0.2$ V

input: logic high has $V_{IH} > 3.7$ V; logic low has $V_{IL} < 1.3$ V

dead zone between 1.3V and 3.7 V

nominal threshold: $V_T = 2.5$ V



Chips with HCT are CMOS with TTL-compatible thresholds

Interfacing CMOS with TTL Logic Family

Interfacing TTL with CMOS Logic Family