Lec-26: Metal Oxide Field Effect Transistors (MOSFETs)
**Structure of MOSFET**

Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET) is the primary component in high-density chips such as memories and microprocessors.

MOSFET is a four terminals FET: **Gate, Source, Drain and body**

**Types of MOSFET:**

- **n-Channel (NMOS)**
- **p-Channel (PMOS)**

- The minimum value of L is referred as the **feature size of the fabrication technology.**
Operation of n channel MOSFET

Body and source are tied to ground. When $V_{DS} = 0$ and $V_{GS} = 0$, source-body and drain-body diode are off hence no current can flow & MOSFET is in cutoff.

When $V_{DS} = 0$ and $0 < V_{GS} < V_t$, Vertical electric field established. Holes repelled and depletion region under gate oxide forms.

When $V_{DS} = 0$ and $V_{GS} > V_t$, A n type inversion layer formed underneath the gate oxide when $V_{GS}$ reaches a critical value $V_t$, called threshold voltage. The channel connects source to drain and current flow between them.
Operation of n channel MOSFET

- When $V_{GS} > V_t$ and a small $V_{DS}$ is applied  
  - Current flows from D to S (Electrons flow from S to D) and $I_{DS} \propto V_{DS}$

Electric field in the oxide is highest at the source end of channel. Thus many electrons are injected near the source. Electric field in the oxide is lowest at the drain end of channel. Thus few electrons are induced near the drain.

- Increasing $V_{GS}$ above $V_t$ increases the electron density in the channel, and in turn increases the conductivity between D & S, hence $I_{DS}$ increases.

- MOSFET behave like a voltage controlled resistor.
Operation of n channel MOSFET

- Increase $V_{DS}$ → Decrease $V_{GD}$ → less electrons at the drain side of the channel

- When $V_{DS} \geq V_{GS} - V_t$ then $V_{GD} \leq V_t$ so no channel exists at the drain side. The channel “pinches-off”

- When channel pinches off, electrons still flows from S to D
  - Electrons are diffused from the channel to the depletion region near D, where they are drifted by the lateral $E$-field to the D

- Further increase of $V_{DS}$ - no effect on the channel - current is “saturated” and the transistor is in “Saturation Mode”
I-V Characteristics of n channel MOSFET

➤ MOS structure looks like a parallel plate capacitor and \( V_{GC} \) is composed of two components: \( V_t \) to form the channel and \( (V_{GC}-V_t) \) to accumulate negative charges in the channel.

\[
Q_{\text{channel}} = CV
\]

\[
C = \frac{\varepsilon_{ox} LW}{t_{ox}} = C_{ox} LW
\]

\[
V = V_{GC} - V_t = \left( \frac{V_{GS} - V_{DS}}{2} - V_t \right)
\]

\[
v = \mu_n E = \mu_n \frac{V_{DS}}{L}
\]

\[
t = \frac{L}{v} = \frac{L^2}{\mu_n V_{DS}}
\]

Charge is carried by electrons and Carrier velocity \( v \) is proportional to the lateral E-field between S and D.
I-V Characteristics of n channel MOSFET

In the Linear region, drain current depends on
– How much charge is in the channel
– How fast the charge is moving

\[ I = \frac{Q_{\text{channel}}}{t} \]

\[ I = \frac{\mu_n C_{ox} W}{L} \left[ (V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \]

For \( V_{GS} > V_t \) and \( V_{DS} \geq V_{dsat} = V_{GS} - V_t \): \( I_D \) is independent of \( V_{DS} \)

In Saturation mode

\[ i_D = \frac{1}{2} \left( \frac{\mu_n C_{ox}}{L} \right) W \left( V_{GS} - V_t \right)^2 \]
Depletion and Enhancement mode MOSFET

- A depletion-type MOSFET has a built-in channel by fabrication i.e. It is ON when no gate-source voltage is applied and need to apply a negative $V_{GS}$ to turn off device. $V_t$ is negative for NMOS.

- MOSFET is said to be enhancement type if gate-source voltage is applied to turn on the transistor. $V_t$ is positive for NMOS.
The effective channel length $L$ is reduced by $\Delta L$ and hence $I_{DS}$ increases.
P-channel MOSFET (PMOS)
Complimentary MOSFET (CMOS)

Complementary MOS or CMOS integrated-circuit technologies provide both NMOS and PMOS on a same IC
Supplement slide: How inversion layer forms?

(1) \( V_G = 0 \) (Equilibrium) 
\( (E_F = \text{constant throughout structure}) \)

Supplement slide: Accumulation ($V_G < 0$)

(2) When $V_G < 0$ (Accumulation): Gate bias is –ve so $E_f$ at the gate goes up. Since M and S have much higher conductivity than O so voltage between Gate and channel mostly drops at oxide. An Electric field will be generated at oxide.

Recall that

$$p(x) = n_i e^{(E_i - E_F)/kT}$$  \hspace{1cm} (1)

$p(x)$ increases near the surface $\rightarrow$ Accumulation (i.e. we have an accumulation of holes near the surface)

Definition of surface potential = $\Phi_S$

Surface potential energy = $e \Phi_S = \text{difference of bulk value of } E_i \text{ and surface value of } E_F$

Supplement slide: Accumulation ($V_G < 0$)

When bands bend upwards:

$$E_i^{\text{bulk}} - E_i^{\text{surface}} = e\Phi_S < 0$$

When bands bend downwards:

$$E_i^{\text{bulk}} - E_i^{\text{surface}} = e\Phi_S > 0$$

Under flatband conditions:

$$\Phi_S = 0$$

Introducing dependence of the potential $\Phi$ on the position $x$:

$$e \Phi(x) = E_i^{\text{bulk}} - E_i(x)$$

$$\Phi_S = \Phi(x = 0)$$

\[ p(x) = n_i e^{(E_i - E_F) / kT} \]

\[ = n_i e^{[E_i^{\text{bulk}} - e\Phi(x) - E_F] / kT} \]

\[ = n_i e^{(E_i^{\text{bulk}} - E_F) / kT} e^{-e \Phi(x) / kT} \]

\[ p(x) = p_0 e^{-e \Phi(x) / kT} \]

Since $\Phi(x) < 0$, $p(x)$ increases close to the surface.
That is, we have accumulation.

Supplement slide: Depletion ($V_G > 0$)

(3) $V_G > 0$ (Depletion)

The gate bias is positive. $E_F$ "goes down" in the metal.

Band diagram:

The depletion layer thickness follows from Poisson's equation:

$$W_D = \sqrt{\frac{2e}{e N_A}} \Phi_S$$  \hspace{1cm} (8)

$E_F$ is near $E_i$ at the surface.

$\Rightarrow$ Semiconductor is practically intrinsic at the surface.

Recall Eq. (7): $p(x) = p_0 e^{-e\Phi(x)/kT}$

It is $\Phi(x) > 0 \Rightarrow p < p_0$, that is, we have a depleted layer near the surface.

Supplement slide: Inversion \((V_G \gg 0)\)

(4) \(V_G \gg 0\). \(\text{Onset of strong inversion}\)

The gate bias is position.

\(E_F\) goes further down in metal.

Semiconductor is depleted of holes near surface.

\(E_F\) is closer to \(E_C\) than to \(E_V\) at the surface.

\(\rightarrow\) Semiconductor is \text{n-type} near surface

\(\rightarrow\) Conductivity type of semiconductor is inverted.

Criterion for the \text{onset of strong inversion}:

\[
e\Phi_S = 2e\Phi_F \quad \text{(Onset of strong inversion)}
\]

where

\[
e\Phi_F = E_i^{\text{bulk}} - E_F^{\text{bulk}}
\]

\(\Phi_S\) means that the semiconductor is as strongly \text{n-type} at the surface as it is \text{p-type} in the bulk.

Using Boltzmann statistics

\[
p = n_i e^{(E_i - E_F)/kT}
\]

and Eqs. (9) and (10), one obtains

\[
e\Phi_S = 2e\Phi_F = 2kT \ln \frac{N_A}{n_i} \quad \text{(Onset of strong inversion)} (12)
\]

At the onset of strong inversion, an \text{n-channel} begins to be formed at the semiconductor surface.