Analog & Digital Electronics

Course No: PH-218

Lec-26: Field Effect Transistors (FETs)

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Field Effect Transistors (FETs)

- Field effect transistors are unipolar device because current is carried by only one type of carriers (majority carriers) while BJTs were bipolar.

- FETs are voltage controlled device where output current is controlled by voltage between two terminals gate and source while BJTs were current controlled device.

- FETs are characterized by very high input resistance (in mega ohm) while BJT have high gain.

- **FETs are less sensitive to temperature variations and are more easily integrated on ICs.**

Types of FETs:

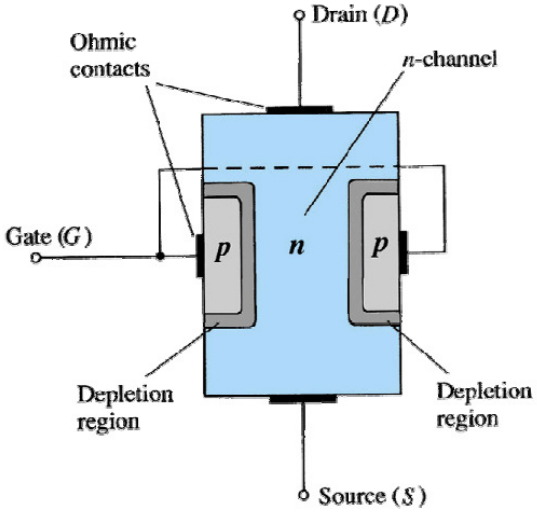
Junction Field Effect Transistor (JFET)

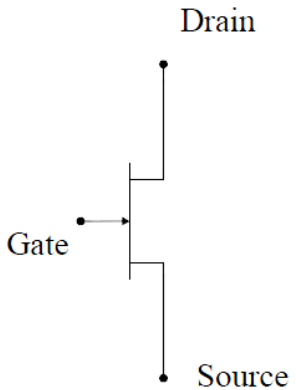
Metal Oxide semiconductor Field Effect Transistor (MOSFET)

Junction Field Effect Transistors (JFETs)

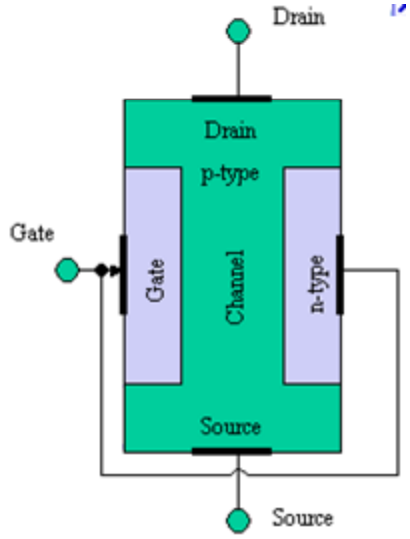
- Junction field effect transistor (JFET) is a type FET that operates with a reverse biased p-n junction to control current in a channel.

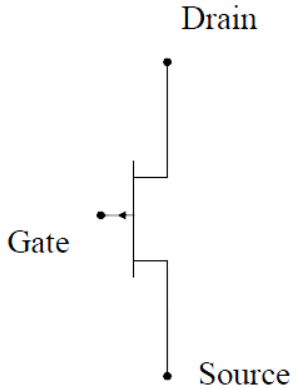
- Depending on the structure, JFET fall in two categories: n channel and p channel JFET





n-channel JFET





p-channel JFET

Operation of n channel FET

Case I: JFET at V_{GS}=0 and V_{DS} > 0

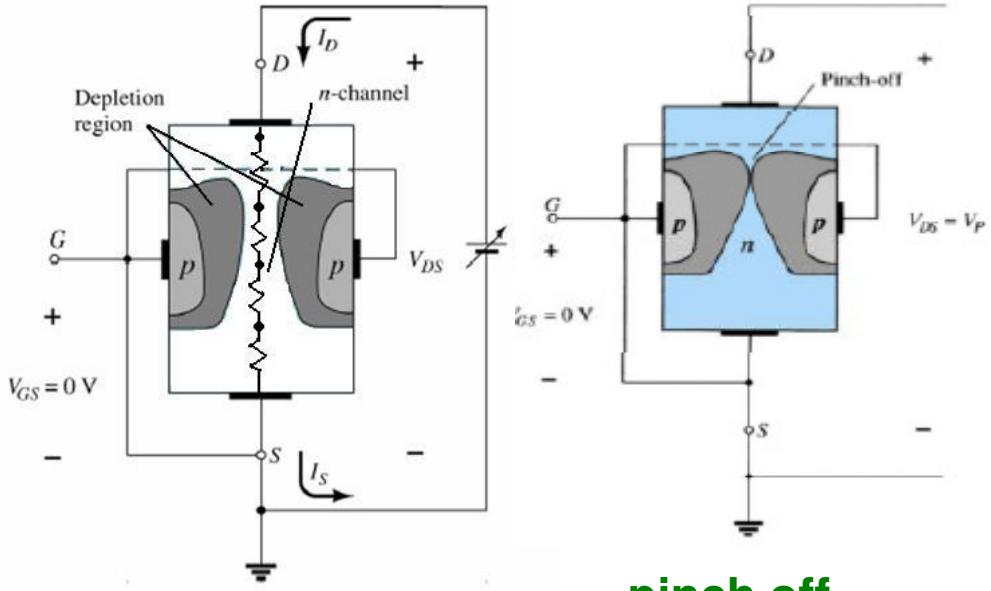
➢ JFET has two p-n junction. When V_{GS}=0 , both gate and source are at same potential so depletion region in low end of each p material is similar.

➢The depletion region is wider near the top of both p type material because of higher potential at upper region. (Upper end of n-channel (drain) is at V_D and lower end (source) is at ground)

The instant V_{DS} is applied across the channel, the electrons are drawn towards the drain giving drain current.

As the V_{DS} is increased from 0V to a few V, the current will increase according to Ohm's law.

As the V_{DS} approaches to V_p, the depletion width increases causing a reduction in channel width.

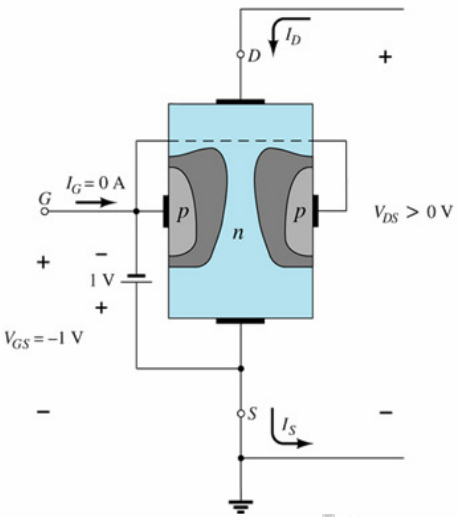


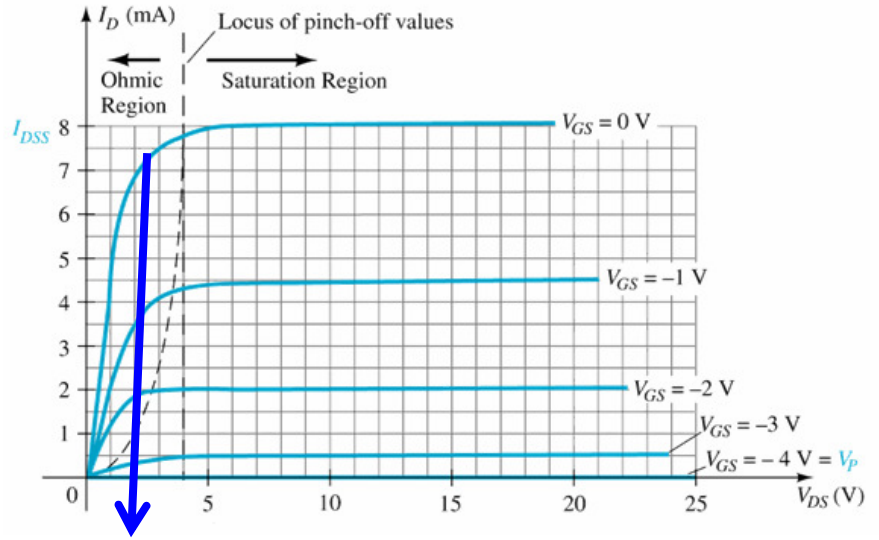
pinch off

The value of V_{DS} (at V_{GS}=0) for which two depletion region touches is called pinch off voltage and denoted by V_P .

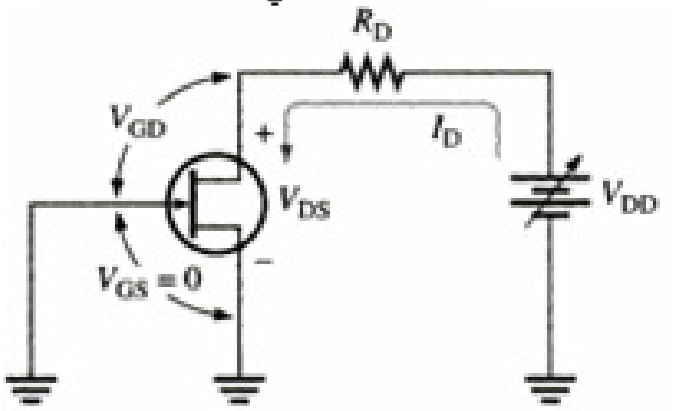
Operation of n channel FET

Case II: JFET at $V_{GS} < 0$ and $V_{DS} > 0$

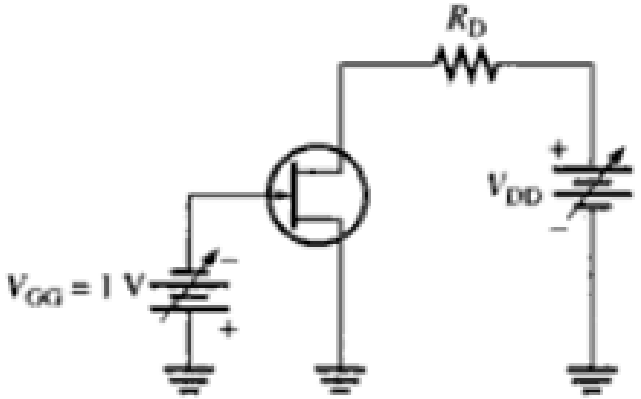




Channel narrowing effect



at V_{GS}=0 and $V_{DS} > 0$



at $V_{GS} < 0$ and $V_{DS} > 0$

The level of V_{GS} that results in $I_D = 0$ mA is $V_{GS} = V_P$

Vp is a negative voltage for n-channel and positive for p-channel JFETs.

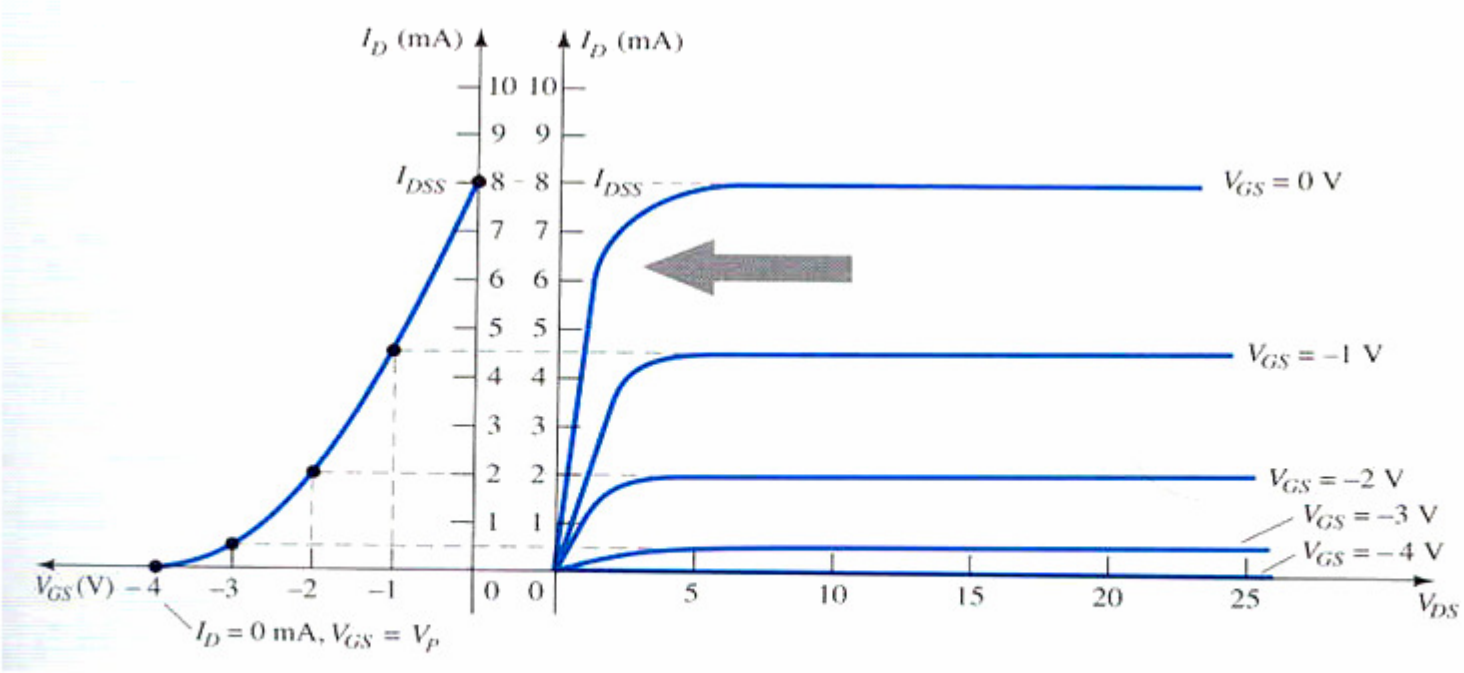
Transfer Characteristics

The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

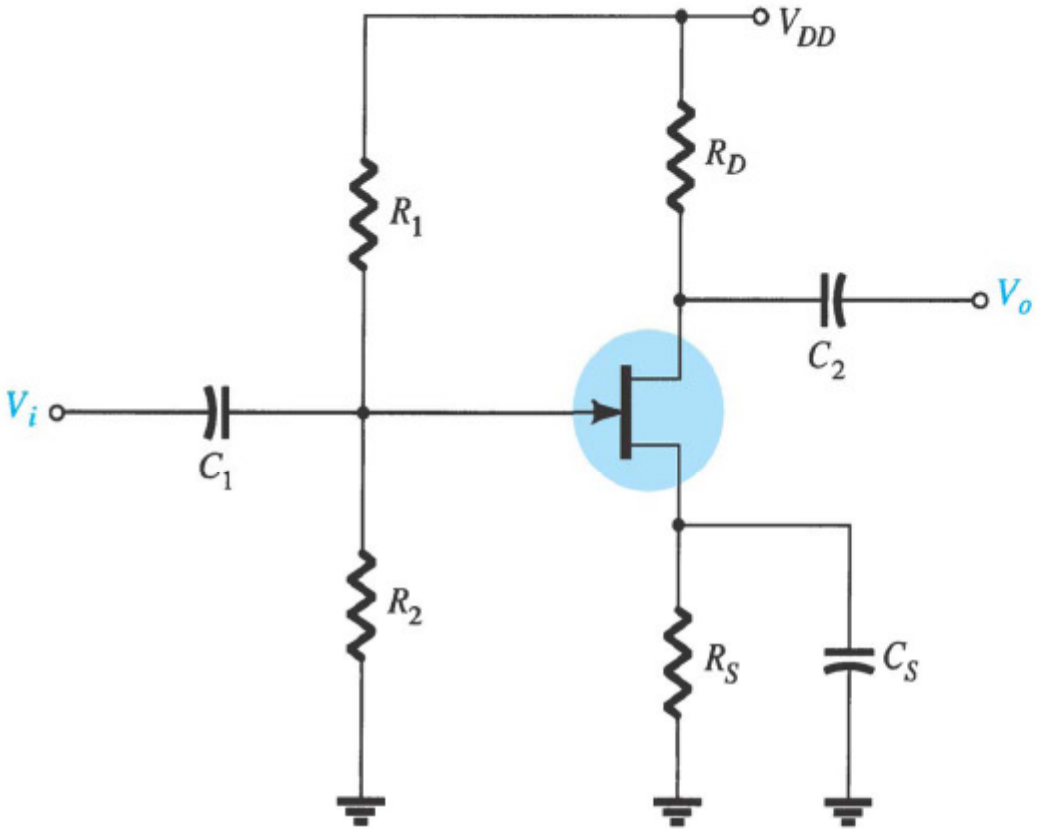
Where I_{DSS} and V_P are constants and V_{GS} is variable and controllable

The transfer function curve may be plotted from the characteristic curve, as shown. Notice the parabolic shape due to the square term relationship between I_D and V_{GS}



Remember that, when $V_{GS} = 0$, $I_D = I_{DSS}$ and when $V_{GS} = V_P$, $I_D = 0$ mA

Biasing scheme of FET: Voltage divider Bias



$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}$$

$$V_{GS} = V_G - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

Biasing schemes for FETs are similar to BJT. Most popular voltage divider scheme is shown here.