Analog & Digital Electronics

Course No: PH-218

Lec-25: Applications of Operational Amplifiers

Course Instructor:

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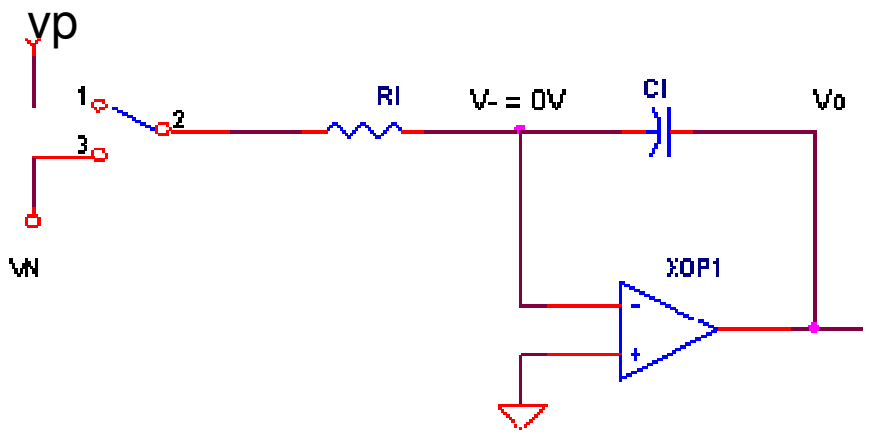
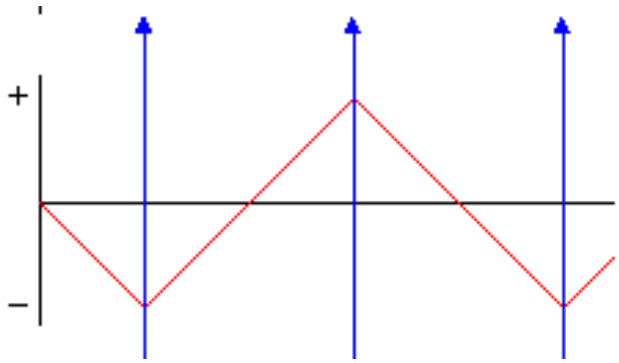
Triangular Oscillator using Op-AMP

When the switch is at position, positive voltage Vp is applied at the input of an integrator and negative linear ramp is developed at the output.

In this case a constant current (I_1) flows from V_p to V_- and charge the C_1 through R_1. Now V_o ramps down linearly. $I_1 = V_p/R_1$; and $\Delta V_o = -(V_p / R_1 C_1)\Delta t$

When the switch is connected at position 3, negative voltage V_N is applied at the input of an integrator and positive linear ramp is developed at the output. In this case V_o ramps up linearly. $I_1 = V_N/R_1$; and $\Delta V_o = -(V_N / R_1 C_1)\Delta t$





Ramp Up: $\Delta Vo / \Delta t = - V_N / (C_1 \cdot R_1)$

Ramp Down: $\Delta Vo / \Delta t = - V_P / (C_1 \cdot R_1)$

Triangular Oscillator using Op-AMP

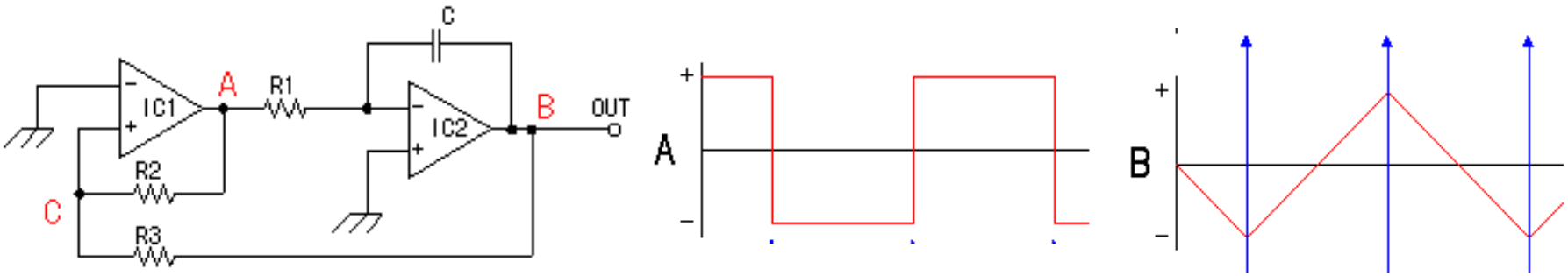
Here the comparator performs the switching action.

Initially assume that output voltage of comparator (at point A) is at its maximum positive level, thus producing negative linear ramp up at integrator output at B.

When the negative linear ramp up voltage reaches lower trigger point (VLTP), comparator will switches to maximum negative level.

This negative voltage will produce positive linear ramp up at integrator output.

This ramp-up continues until voltage reaches to upper trigger point (VUTP) and at this point comparator will switch again to maximum positive level.



VUTP= +VCC · R3 / R2

VLTP = - VCC · R3 / R2

Voltage Controlled Oscillator (VCO)

Voltage controlled Oscillator is based on the principle of Varactor. VCO is an oscillator whose frequency can be changed by a variable dc control voltage.

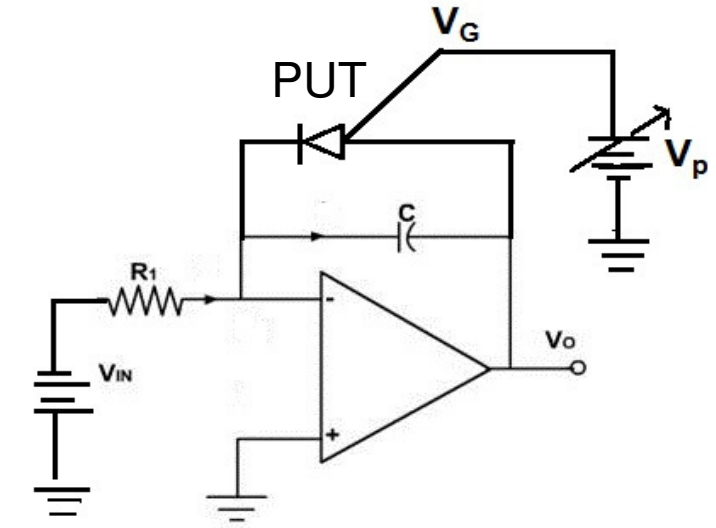
Voltage controlled saw-tooth oscillator can be built by connecting a switching device (PUT) in parallel with the feedback capacitor of an op-amp integrator.

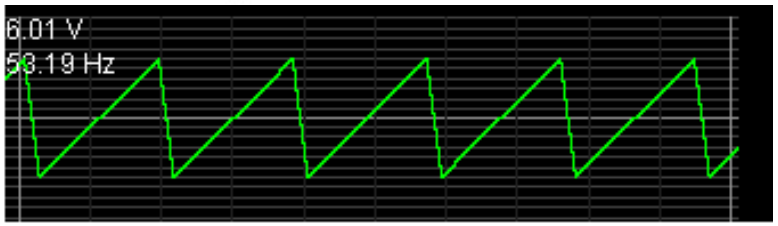
PUT is a programmable unijunction transistor with an anode, a cathode and a gate terminal.

The gate is always biased positive with respect to cathode.

When the anode voltage exceeds the gate voltage by 0.7V, the PUT turns on and act as forward bias diode.

When the anode voltage falls below this level, the PUT turns off.





Operation of Voltage Controlled Oscillator

Application of negative V_{in} at op-amp integrator produces positive linear ramp at the output. During the time ramp is increasing, the circuit acts as a integrator.

The PUT turns on when the output ramp (at anode) exceeds the gate voltage by 0.7V. The gate is set to the desired sawtooth peak voltage.

When the PUT turns on, capacitor start discharging until PUT's forward voltage V_F. Discharge continues until the PUT current falls below the holding value. At this point PUT turns off and capacitor begins to charge again, thus generating a new output ramp up.

The cycle continually repeats, and the resulting output is a repetitive sawtooth waveform.

The frequency of oscillation is determined by the R_1C time constant of the integrator and the peak voltage set by the PUT gate voltage.

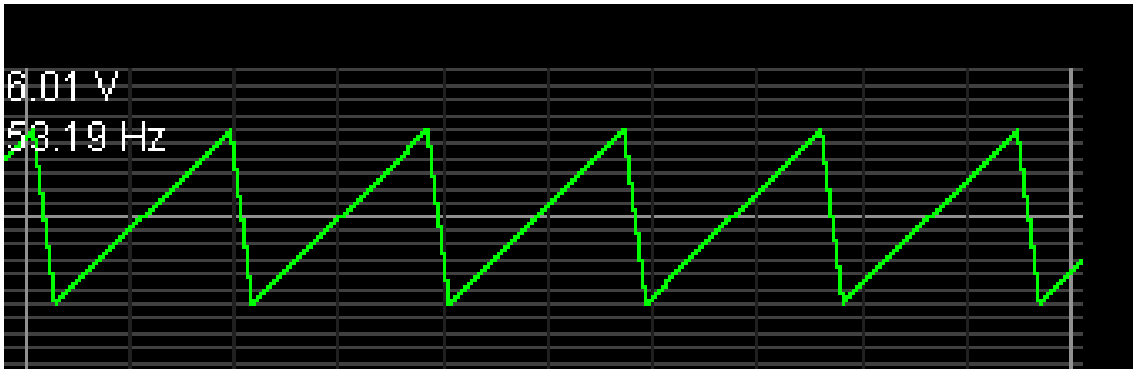
Frequency of Voltage Controlled Oscillator

Charging rate of capacitor = V_{in} / R_1C

Time taken to charge the capacitor from V_F to V_p = T (time period)
Here we neglected the rapid discharge time.

$$T = \frac{(V_p - V_F)}{V_{in} / R_1 C}$$

$$f = \frac{V_{in}}{R_1 C} \frac{1}{(V_p - V_F)}$$

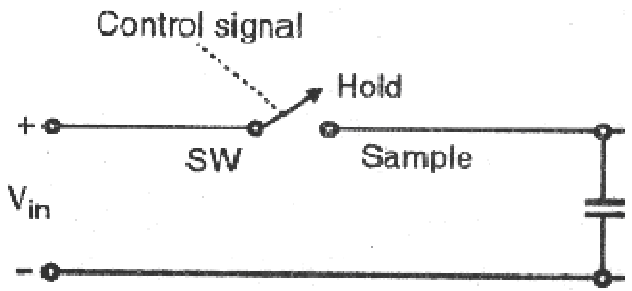


Sample and Hold Circuit

The sample & hold circuit is used to hold the sampled value of the input signal for a specified period of time. Thus S/H operation has two different processes: sampling the input signal and holding the latest sample value

Sampling Mode: In this mode, the switch is in the closed position and the capacitor charges to the instantaneous input voltage.

Holding Mode: In this mode, the switch is in the open position. The capacitor is now disconnected from the input. As there is no path for the capacitor to discharge, it will hold the voltage on it just before opening the switch. The capacitor will hold this voltage till the next sampling instant.



Basic sample and hold

Sample and Hold Circuit

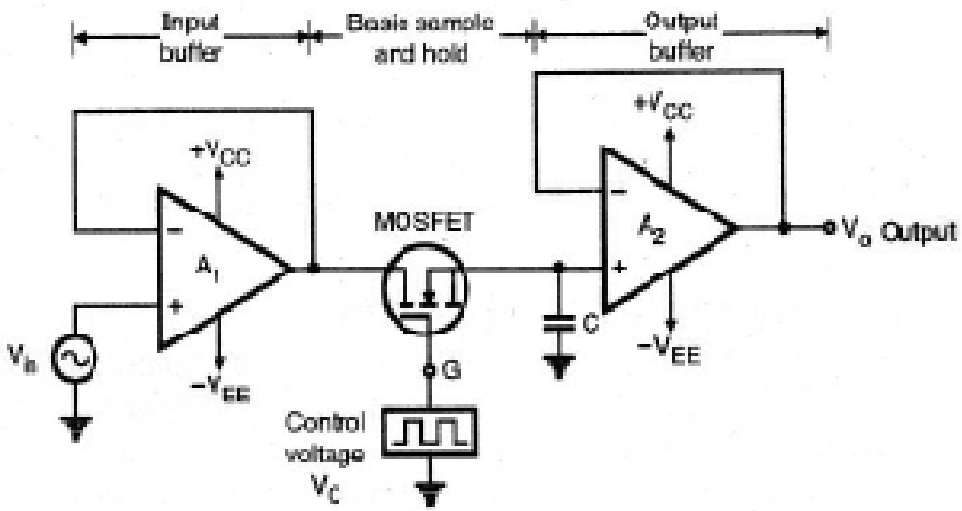
All high quality sample-and-hold circuits must meet certain requirements:

1. The holding capacitor must charge up and settle to its final value as quickly as possible.

2. When holding, the leakage current at the capacitor must be as near zero as possible to minimize voltage drift with time.

The negative pulse at the gate of p-channel MOSFET will turn the switch on and the holding capacitor will charge with a time constant $R_{on}C$ to the instantaneous value of input voltage.

In the absence of –ve pulse, the switch is off and capacitor is isolated from output, thus holding the voltage.



Sample and hold circuit using OP-AMP

Characterization Parameters of an Op-Amp

Output Offset Voltage:

In an OPAMP even if the input voltage is zero an output voltage can exist.
There are two main cause of this unwanted offset voltage.
Input offset voltage.
Input offset current.

1.Input Offset Voltage:

Input offset voltage is defined as the voltage that must be applied between the two input terminals of an OPAMP to null or zero the output .
The smaller the input offset voltage the better the differential amplifier, because its transistors are more closely matched. Typical value is around 6mV.

2.Input Offset Current:

The input offset current I_{io} is the difference between the currents into inverting and non-inverting terminals of a balanced amplifier. $I_{io} = | I_{B1} - I_{B2} |$

The I_{io} for the 741C is 200nA maximum.

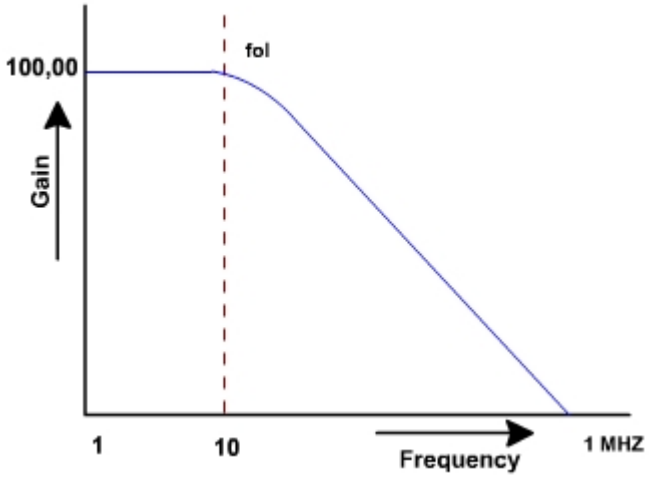
Characterization Parameters of an Op-Amp

Input Voltage Range :

Input voltage range is the range of a common mode input signal for which a differential amplifier remains linear. It is used to determine the degree of matching between the inverting and non-inverting input terminals. For the 741C, the range of the input common mode voltage is ± 13V maximum.

Gain Bandwidth Product:

The gain bandwidth product is the bandwidth of the OPAMP when the open loop voltage gain is reduced to 1. From open loop gain vs frequency graph, It can be found that for the 741C OPAMP, the gain reduces to 1 at 1 MHz frequency . The mid band voltage gain is 100, 000 and cut off frequency is 10Hz.



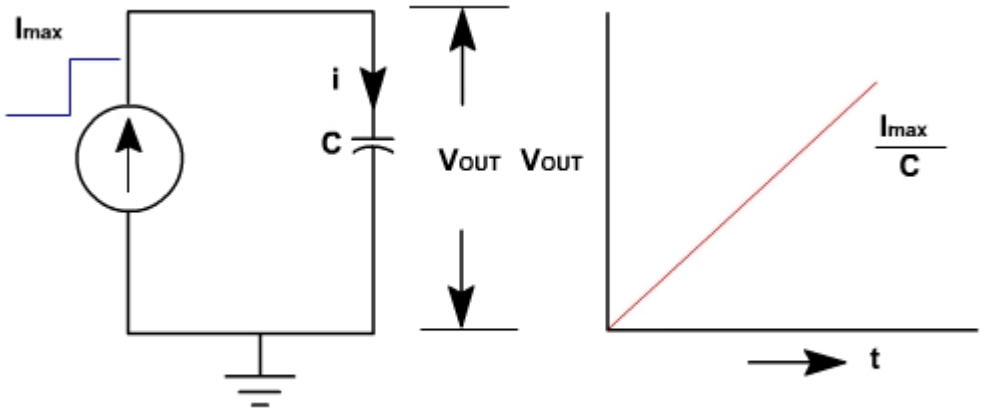
Characterization Parameters of an Op-Amp

Slew rate:

Slew rate is defined as the maximum rate of change of output voltage per unit of time under large signal conditions and is expressed in volts / μsecs.

$$SR = \left(\frac{dV_o}{dt}\right)_{\max}$$

$$i = C\frac{dV}{dt} \qquad \frac{dV}{dt} = \frac{i}{C}$$



Slew rate indicates how rapidly the output of an OPAMP can change in response to changes in the input frequency with input amplitude constant. The slew rate changes with change in voltage gain and is normally specified at unity gain.

If the slope requirement is greater than the slew rate, then distortion occurs. For the 741C the slew rate is low 0.5 V / mS. which limits its use in higher frequency applications.