Analog & Digital Electronics

Course No: PH-218

Lec-22: Differential Amplifiers

Course Instructor:

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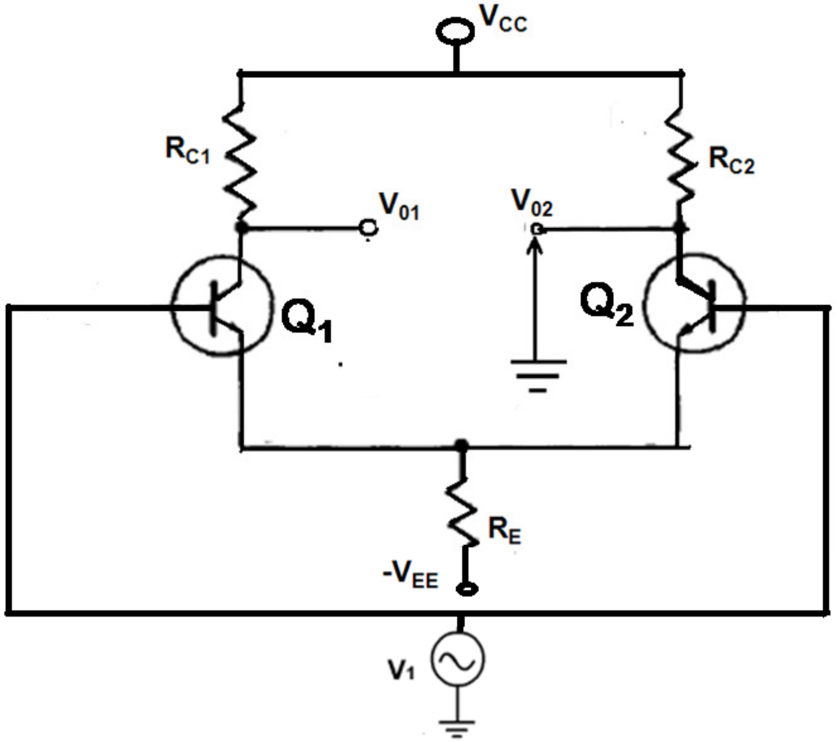
Common Mode Rejection Ratio (CMRR)

$$I_b = \frac{v_1 - 2(\beta+1)I_b R_E}{r_\pi}$$

$$I_b = \frac{v_1}{r_\pi + 2(\beta+1)R_E}$$

$$V_{o1} = I_c R_c = \frac{\beta v_1 R_C}{r_\pi + 2(\beta+1)R_E}$$



$$\boxed{A_c = \frac{V_{o1}}{v_{i1}} = \frac{\beta R_C}{r_\pi + 2(\beta+1)R_E}}$$

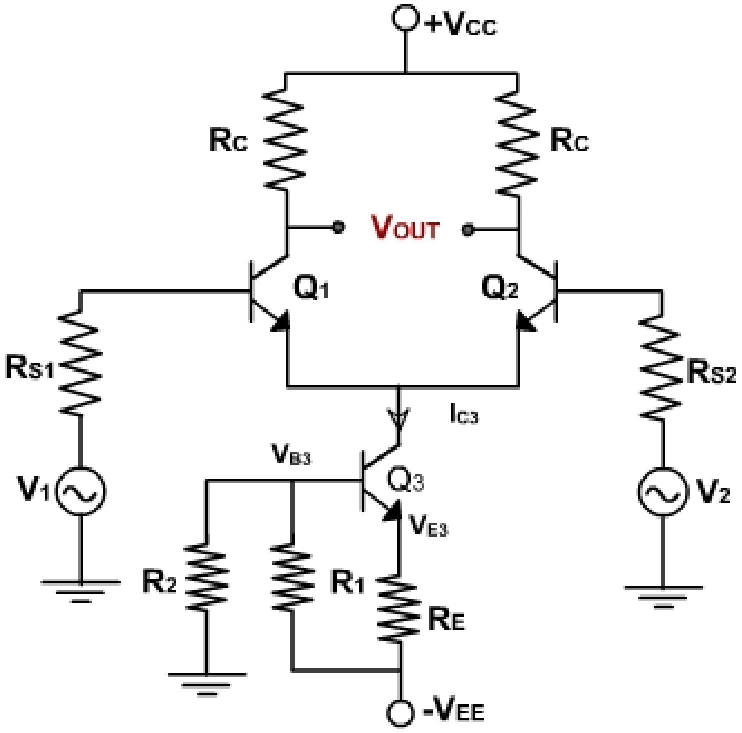
$$\boxed{\mathrm{CMRR} = \frac{|\mathrm{A_d}|}{|\mathrm{A_c}|}}$$

To get high CMRR, the value of emitter resistance should be very high.

Larger the CMRR, better is the differential amplifier.

Constant Current Source

The CMRR of a DA can be improved by making the common mode gain as small as possible (high R_E). One popular method to increase the ac value of R_E is using Constant current source circuit.



The resistance R_E is replaced by constant current transistor Q_3. The dc collector current in Q_3 is established by R_1, R_2, & R_E.

$$V_{B3} = \frac{R_2}{(R_1 + R_2)}(-V_{EE})$$

$$V_{E3} = V_{B3} - V_{BE3} = \frac{-R_2}{(R_1 + R_2)} V_{EE} - V_{BE3}$$

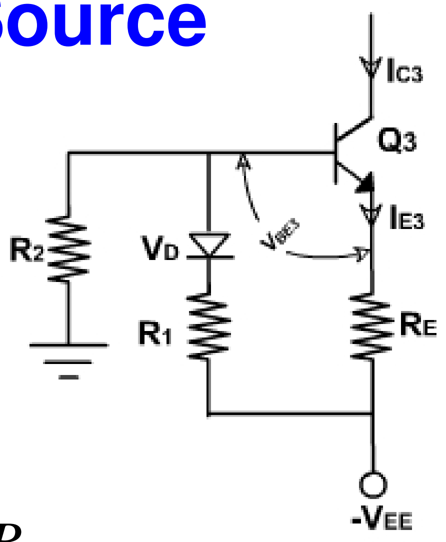
$$I_{E3} = I_{C3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

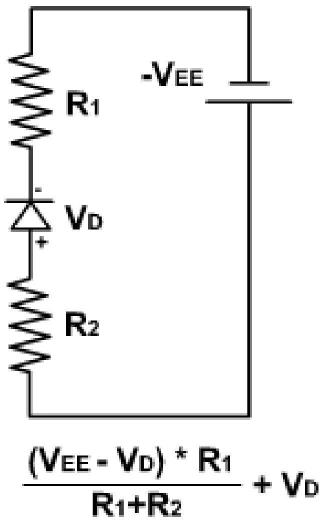
$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left[\frac{R_2}{R_1 + R_2} V_{EE}\right] - V_{BE3}}{2R_E}$$

The collector current, I_{C3} in transistor Q_3 is fixed because no signal is injected into either the emitter or the base of Q_3 therefore supplying constant emitter current.

The internal resistance of constant current source is very high (ideally infinite) hence we get very high R_E without physically increasing the value of R_E

Modified Constant Current Source





If temperature changes, V_{BE} changes and current I_E also changes.

To improve thermal stability, a diode is placed in series with resistance R_1. This helps to hold the current I_{E3} constant even though the temperature changes.

KVL law at base of Q3: $(V_{EE} - V_D)\dfrac{R_1}{(R_1+R_2)} + V_D = V_{BE3} + I_{E3}R_E$

$$I_{E3} = \frac{1}{R_E}\left\{\frac{R_1}{(R_1+R_2)}V_{EE} + \frac{R_2}{(R_1+R_2)}V_D - V_{BE3}\right\}$$

If R_1 and R_2 are chosen in such as way that

$\dfrac{R_2}{(R_1+R_2)}V_D = V_{BE3}$ then $\boxed{I_{E3} = \dfrac{1}{R_E}\dfrac{R_1}{(R_1+R_2)}V_{EE}}$

Since the cut – in voltage V_D of diode approximately the same value as the base to emitter voltage V_{BE3} of a transistor the above condition cannot be satisfied with one diode. Hence two diodes are used in series for V_D.

Current Mirror

The circuit in which the output current is forced to equal the input current is said to be a current mirror circuit. Thus in a current mirror circuit, the output current is a mirror image of the input current.

Since Q3 and Q4 are identical transistors the current and voltage are

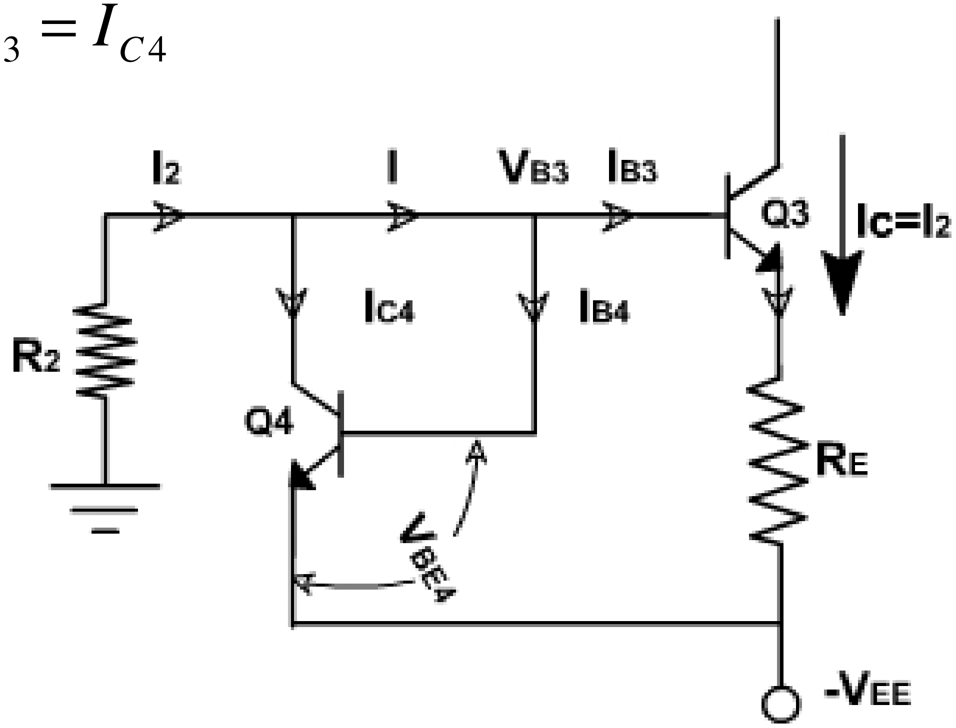
$$V_{BE3} = V_{BE4} \qquad I_{B3} = I_{B4} \qquad I_{C3} = I_{C4}$$

$$I_2 = I_{C4} + I = I_{C3} + I$$

$$I = I_{B3} + I_{B4} = 2I_{B3}$$

$$I_2 = I_{C3} + 2I_{B3}$$

$$\boxed{I_2 = I_{C3}\left(1 + \frac{2}{\beta_{dc}}\right) \cong I_{C3}}$$



Generally β_{dc} is very large enough, therefore 2/ β_{dc} is small and so ignored.

Summary : Differential Amplifier

- **If the differential amplifier is double ended input and double ended output then voltage gain**

$$\boxed{A_d = \frac{v_o}{v_i} = \frac{R_C}{r_e}}$$

Where $v_i = v_{i1} - v_{i2}$

- **For a single ended input voltage gain is given by**

$$\boxed{v_o = \frac{R_C}{2r_e}(v_1)}$$

- **For a common mode, gain is given by**

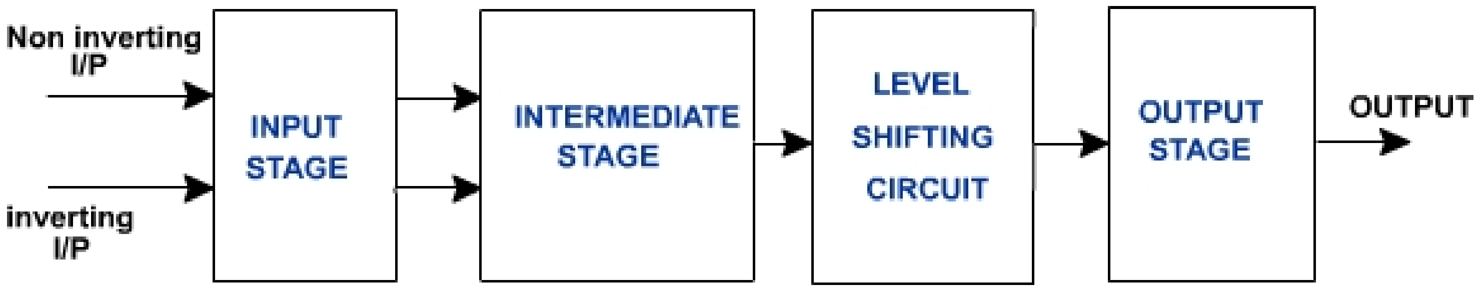
$$\boxed{A_c = \frac{V_{o1}}{v_{i1}} = \frac{\beta R_C}{r_\pi + 2(\beta + 1)R_E}}$$

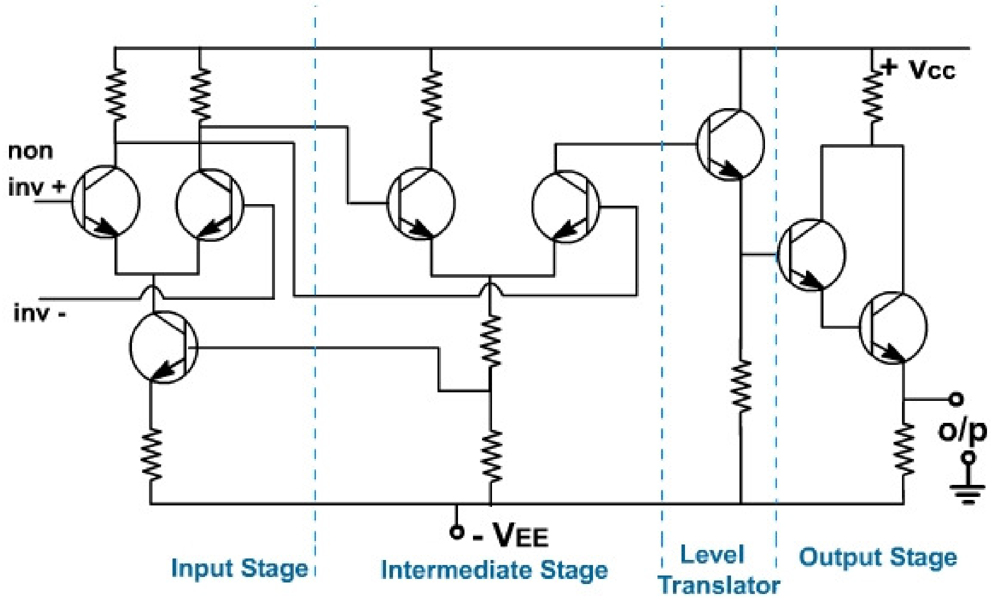
To get high CMRR, the value of emitter resistance should be very high.

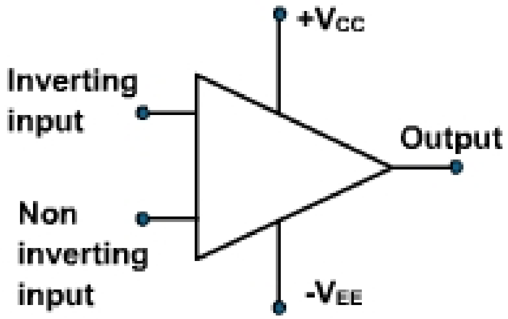
Larger the CMRR, better is the differential amplifier.

Operational amplifier (OP-AMP)

An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential (OPAMP) amplifiers and followed by a level translator and an output stage. An operational amplifier is available as a single integrated circuit package.







Operational amplifier (OP-AMP)

The input stage is a dual input dual output differential amplifier. This stage provides most of the voltage gain of the amplifier and also establishes the input resistance of the OPAMP.

The intermediate stage of OPAMP is another differential amplifier which is driven by the output of the first stage. This is usually dual input single output.

Because direct coupling is used, the dc voltage level at the output of intermediate stage is well above ground potential. Therefore level shifting circuit is used to shift the dc level at the output downward to zero with respect to ground.

The output stage is generally a push pull complementary amplifier. The output stage increases the output voltage swing and raises the current supplying capability of the OPAMP. It also provides low output resistance.

Problem on cascaded DA

For the cascaded differential amplifier shown in **figure** determine:
(a) The collector current and collector to emitter voltage for each transistor.
(b) The overall voltage gain. (c) The input resistance. (d) The output resistance.
Assume that for the transistors used h_{FE} = 100 and V_{BE} = 0.715V

$$I_{E1} = \frac{V_{EE} - V_{BE}}{2R_{E1} + R_{in}/\beta_{dc}}$$

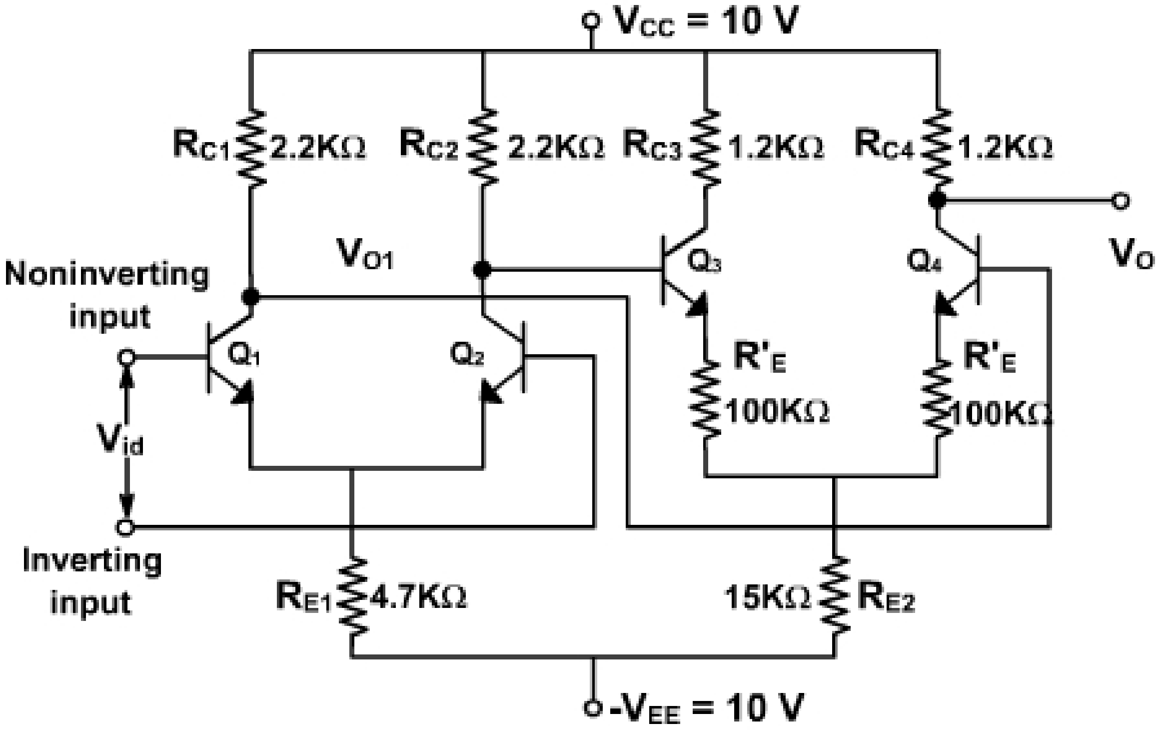
$$= \frac{10 - 0.715}{2 \times 4.7\text{k}\Omega + 0} = 0.988\ \text{mA}$$

$I_{C1} = I_{C2}$ =0.988 mA.

$V_{C1} = V_{CC} = -R_{C1}\ I_{C1}$
= 10 – (2.2kΩ) (0.988 mA)
= 7.83 V = V_{C2}

Since the voltage at the emitter of Q_1 and Q_2 is -0.715 V,

$V_{CE1} = V_{CE2} = V_{C1} - V_{E1}$
= 7.83 + 0715 = 8.545 V



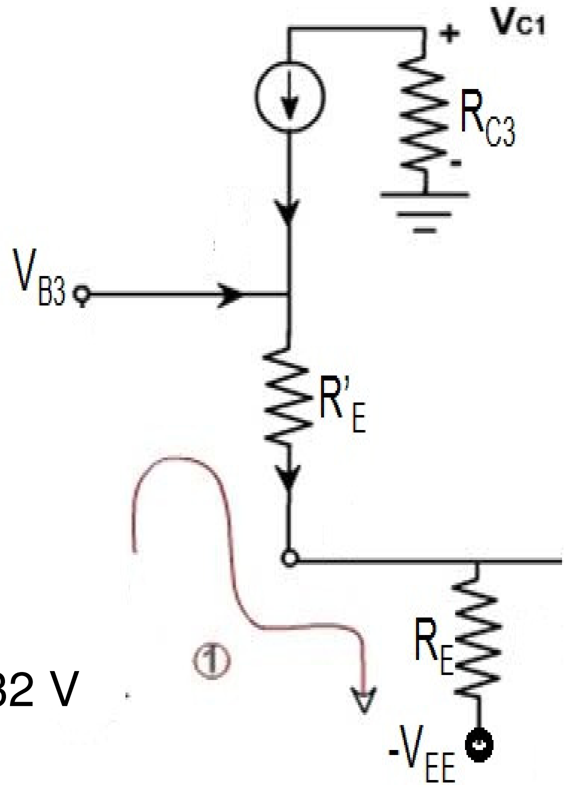
R_E

$-V_{EE}$

Problem on cascaded DA

writing the Kirchhoff's voltage equation for the base emitter loop of the transistor Q_3:

$$V_{B3} = V_{CC} - R_{C2} I_{C2} = V_{BE3} + R'_E I_{C3} + R_{E2} (2 I_{E3}) - V_E$$



$$V_{CC} - R_{C2} I_{C2} - V_{BE3} - R'_E I_{E3} - R_{E2} (2 I_{E3}) + V_{EE} = 0$$

$$V_{CC} - R_{C2} I_{C2} - V_{BE3} - R'_E I_{E3} - R_{E2} (2 I_{E3}) + V_{EE} = 0$$

$$\boxed{I_{E3} = \frac{V_{CC} - R_C I_{C2} - V_{BE3} + V_{EE}}{R'_E + 2R_{E2}} = 0.569\ mA}$$

$I_{C3} = I_{C4} = 0.569$ mA.

$V_{C3} = V_{C4} = V_{CC} - R_{C3} I_{C3} = 10 - (1.2\text{k}\Omega)(0.569\text{ mA}) = 9.32$ V

$V_{CE3} = V_{VCE4} = V_{C3} - V_{E3} = 9.32 - 7.12 = 2.2$ V

(c). The input resistance of the cascaded differential amplifier is the same as the input resistance of the first stage, that is $R_i = 2\beta_{ac}(r_{e1}) = (200)(25.3) = 5.06\text{ k}\Omega$

(d). The output resistance of the cascaded differential amplifier is the same as the output resistance of the last stage. Hence, $R_O = R_C = 1.2\text{ k}\Omega$

Problem on cascaded DA

First, we calculate the ac emitter resistance r'_e of each stage and then its voltage gain.

$$r_{e1}' = \frac{25mV}{I_{E1}} = \frac{25mV}{0.988mA} = 25.3\Omega = r_{e2}'$$

$$r_{e3}' = \frac{25mV}{I_{E3}} = \frac{25mV}{0.569mA} = 43.94\Omega = r_{e4}'$$

The first stage is a dual input, balanced output differential amplifier, therefore, its voltage gain is

$$\boxed{A_{d1} = \frac{v_{o1}}{v_{id}} = \frac{R_{C1} \parallel R_{i2}}{r_{e1}}}$$

$$A_{d1} = \frac{2.2\ k\Omega \parallel 28.79\ k\Omega}{25.3} = 80.78$$

Where R_{i2} = input resistance of the second stage = $2\beta_{ac}\ (r_{e3}+R'_E)$ = 28.79kohm

The second stage is dual input, unbalanced output differential amplifier with swamping resistor R'_E, the voltage gain of which is

$$\boxed{A_{d2} = \frac{v_o}{v_{o1}} = \frac{R_{C4}}{2(R'_E + r_{e4})} = \frac{1.2k\Omega}{287.88} = 4.17}$$

Hence the overall voltage gain is $A_d = (A_{d1})\ (A_{d2}) = (80.78)\ (4.17) = 336.85$